PIXELPLUS CO., LTD.

Preliminary
Data sheet

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

PC3089N

Rev 0.1

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1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ *Revision History*

Version	Date [D/M/Y]	Notes	Writer
0.0	10/10/2013	*(Preliminary)*	Taegu Lee
0.1	12/03/2014	First edition for customer	Sanghyun Han

Caution : This datasheet can be changed without prior notice !! If you want to get up-to-date version, please send a mail to support@pixelplus.co.kr.

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

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1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Features

- ▷ 756 x 512 total pixel array with RGB bayer color filters and micro-lens.
- ▷ Power supply : HVDD/CVDD/AVDD=3.3V or HVDD/CVDD/AVDD=2.8V
- ▷ Input. Clock Frequency : 27MHz
- ▷ Output formats :
  - ◆ Composite Output mode :
    - CVBS (NTSC/PAL),
  - ◆ Digital Output mode :
    - max. D1 (720x480) YCbCr422/RGB565/ RGB444. (progressive, 60 fps @ 54MHz)
    - max. D1 (720x480) Bayer (progressive, 60 fps @ 27MHz)
  - ◆ Analog/Digital Output mode :
    - ITU-R. BT656 (720x240/288) (interlaced, 60 fields @ 27MHz)
    - CVBS (30 fps @ 27MHz)
- ▷ Image processing on chip : lens shading, gamma / defect / color correction, low pass filter, color interpolation, saturation, edge enhancement, brightness, contrast, special effects, auto black level , auto white balance, auto exposure control and back light compensation.
- ▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus.
- ▷ Free scaling(up & down).
- ▷ High Image Quality and Ultra low light performance.
- ▷ I2C,SPI master include.
- ▷ Motion detection support
- ▷ Alarm mode, Privacy mode support
- ▷ Artificial Intelligence power save mode.
- ▷ Chip Address Selection PADs
- ▷ Horizontal / Vertical mirroring.
- ▷ cropping.
- ▷ 50Hz, 60Hz flicker automatic cancellation.
- ▷ Software Reset.
- ▷ External Sync (Gen. Lock) support
- ▷ Smart IR-LED control.
- ▷ Crystal input support.
- ▷ On chip regulator for DVDD.
- ▷ CSP/CLCC/PLCC Package type supports

Parameter	Typical Value
Pixel Size	6.35 um x 7.4 um
Effective Pixel Array	756(H) x 504(V)
Effective Image Area	4.80 mm x 3.73 mm
Optical Format	1/3 inch
Input Clock frequency	27 MHz
Max. Frame Rate	- NTSC : 60 fields/sec - PAL : 50 fields/sec
Dark Signal	50.0[mV/sec] @60℃
Sensitivity	13.2[V/Lux.sec]
Power Supply	Analog : 3.3V(or 2.8V) HVDD : 3.3V(or 2.8V) CVDD : 3.3V(or 2.8V)
Power Consumption	380mW @Dynamic
	363uW @Standby
Operating Temp. (Fully Functional Temp)	-40 ~ 105 [℃]
Dynamic Range	60.7[dB]
SNR	46.5[dB]

[Table 1] Typical Parameters

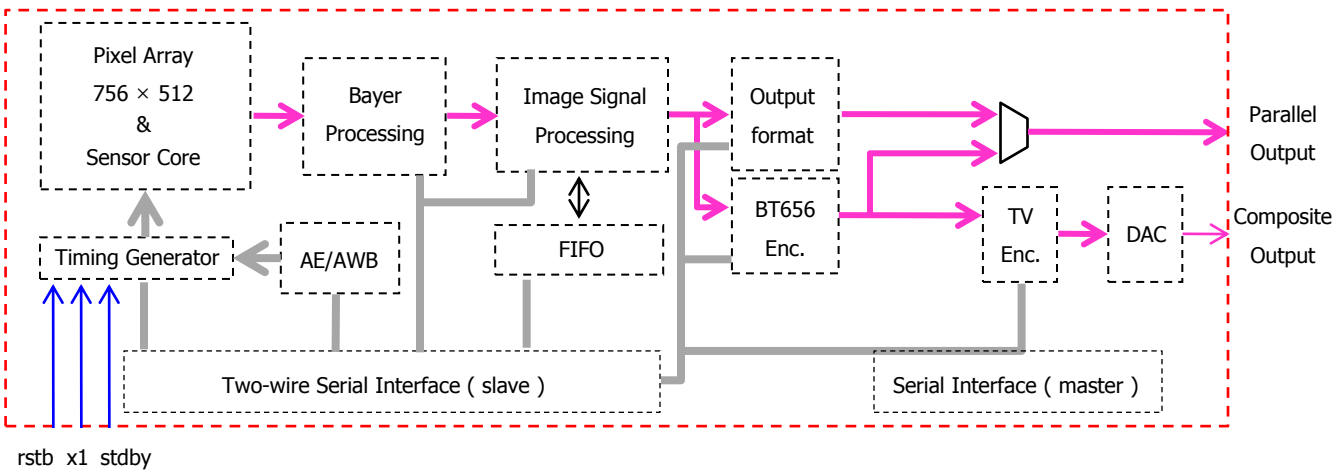
1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ *Signal Environment*

PC3089N don't have tolerant Input pads. The input signal must be equal to HVDD for stable operation. If the power of input signal is higher than recommended , it may flow leakage current by shot circuit path in the input PADs.

▶ *Chip Architecture*

PC3089N has 756 x 512 total pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.



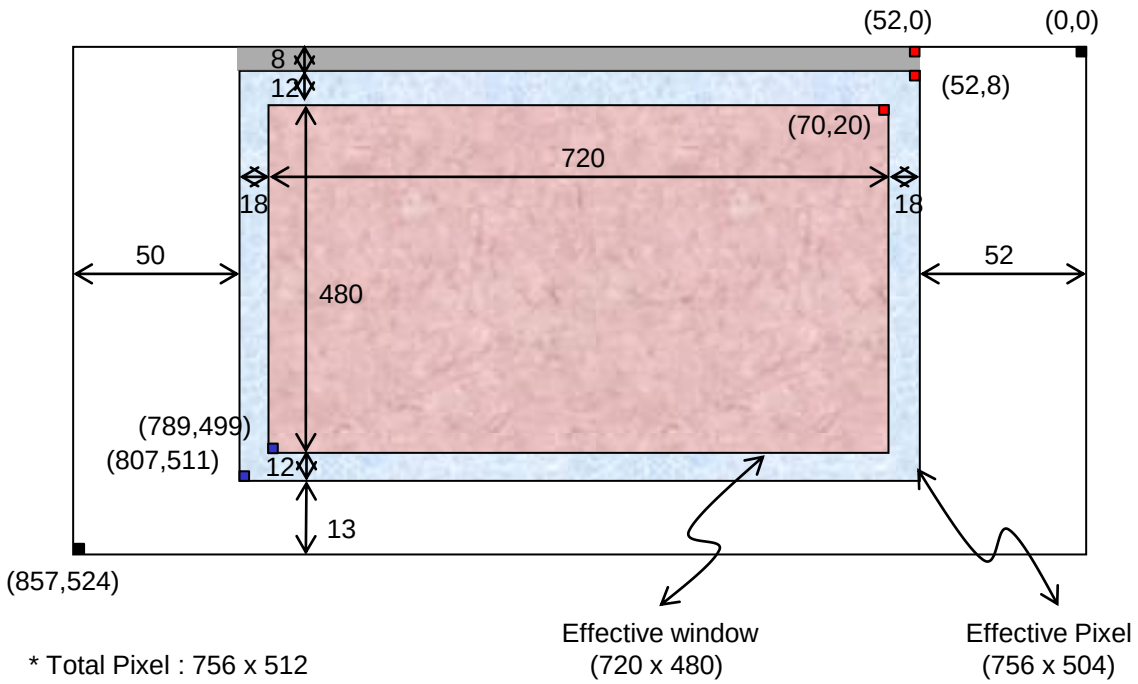
[Fig. 1] Block Diagram

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ *Frame Structure and Windowing*

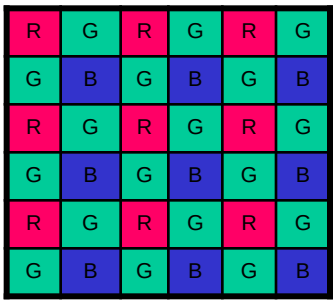
Origin *(0, 0)* of the frame is at the upper right corner. Size of the frame is determined by two registers : *framewidth(Reg.A-06h, A-07h)* and *frameheight(Reg.A-08h, A-09h).* One frame consists of *framewidth + 1* columns and *frameheight + 1* rows. *framewidth* and *frameheight* can be programmed to be larger than total array size. Default window array of 720 x 480 pixels is positioned at *(70, 20).* It is possible to define a specific region of the frame as a window. Pixel scanning begins from *(0, 0)* and proceeds row by row downward, and for each line scan direction is from right to the left. Hsync signal indicates if the output is from a pixel that belongs to the window or not. There are two counters to indicate the present coordinate of frame scanning : Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *frameheight* , and 0 to *framewidth* respectively. The counter values increase at the pace of pixel clock (pclk), which does not change as the frame size is altered. The pixel data rate is fixed and is independent of frame size. [Fig. 2] shows *window x, y start/stop(Reg.A-0Ch ~ A-13h)* registers value for default window and maximum window.

PC3089N Frame Structure



[Fig. 2] Default Data Structure of Frame and Window. (Top View)

▶ Data Formats



[Fig. 3] Bayer Color Filter Pattern

Pixel array is covered by Bayer color filters as can be seen in the [Fig. 3]. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PC3089N provides this Bayer pattern RGB data through an 10bit channel. It takes one pclk to pass one pixel RGB data to output bus. But since it is necessary to know all 3 color components R, G, B to produce a color for a pixel, the other two components must be inferred from other pixel data. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as an average of its four nearest R neighbors. This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PC3089N adopts a low pass filter to prevent the interference patterns (called Moiré pattern) from degrading the image quality too much. After color interpolation, every pixel has all three color components. These three color components R, G, B can be routed to 10 bits output pins in such a way RGB565. It takes two pclk's to pass one pixel RGB data to output bus.

It is possible to extract monochrome luminance data from RGB color components and the conversion equation is : Y = 0.299R + 0.587G + 0.114B where R,G and B are gamma corrected color components. And the color information is separated from luminance information according to following equations.

$$U = 0.492 (B – Y), \quad V = 0.877 (R – Y)$$

Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality.

U1	Y1	V1	Y2	U3	Y3	V3	Y4	…

[Fig. 4] 4:2:2 YUV Data Sequence.

[Fig. 4] shows 4:2:2 YUV data sequence. PC3089N supports 4:2:2 YUV data format where U and V components are horizontally sub-sampled such that U and V for every other pixel are omitted. PC3089N also supports ITU-R BT.601 YC_BC_R format which is a scaled, offset version of YUV. Y is the same in both formats but the C_BC_R is formed as follows.

$$C_B = 0.564 (B – Y) + 128$$
$$C_R = 0.713 (R – Y) + 128$$

▶ Data and Synchronization Timing

1) VGA

[Fig. 5] shows the default data sequence of PC3089N. In [Fig. 5] VSYNC/HSYNC/PCLK polarity can have any combinations possible. Data can be latched at the rising or falling edge of PCLK. HSYNC can be set to be active high or active low. The sequence default YUV data is [U,Y, V, Y, …] for common even / odd rows.

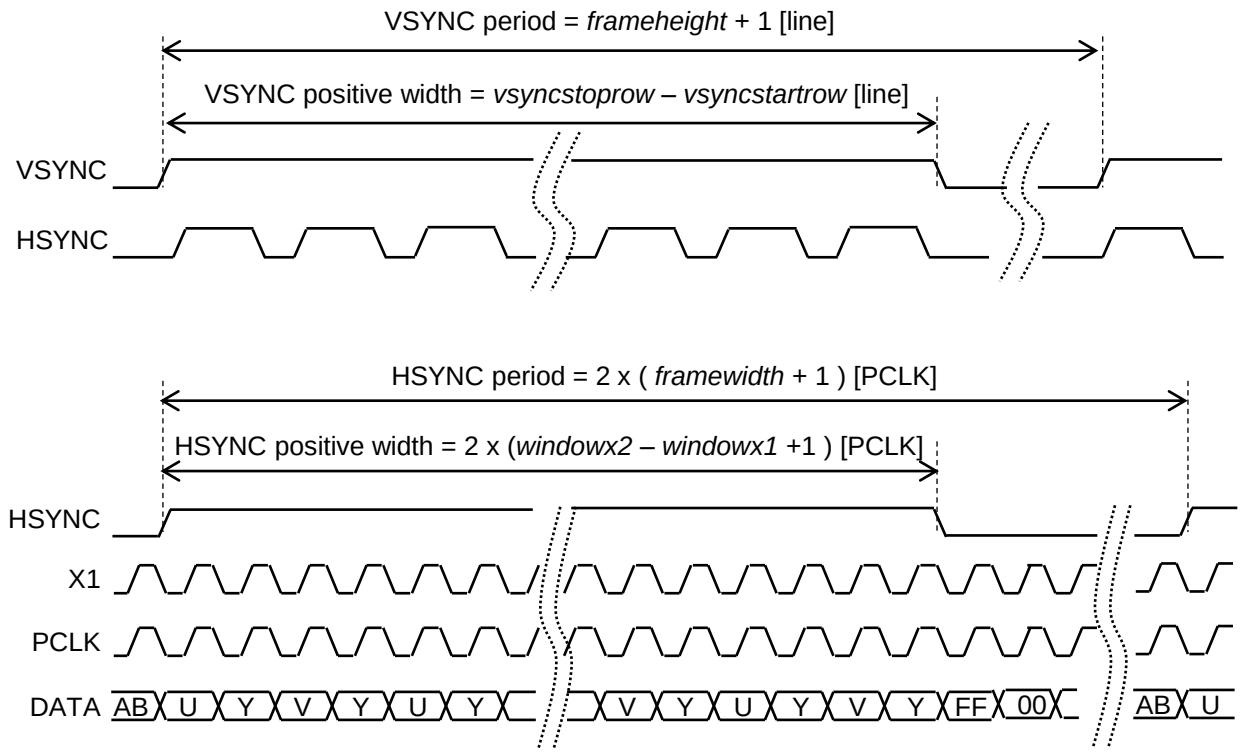
The positive width of VSYNC can be programmed by *vsyncstartrow* and *vsyncstoprow* (register value) and given by

VSYNC positive width = *vsyncstartrow* – *vsyncstoprow* [line]

The positive width of HSYNC can be programmed by *windowx1 / x2(Register Value)* and given by

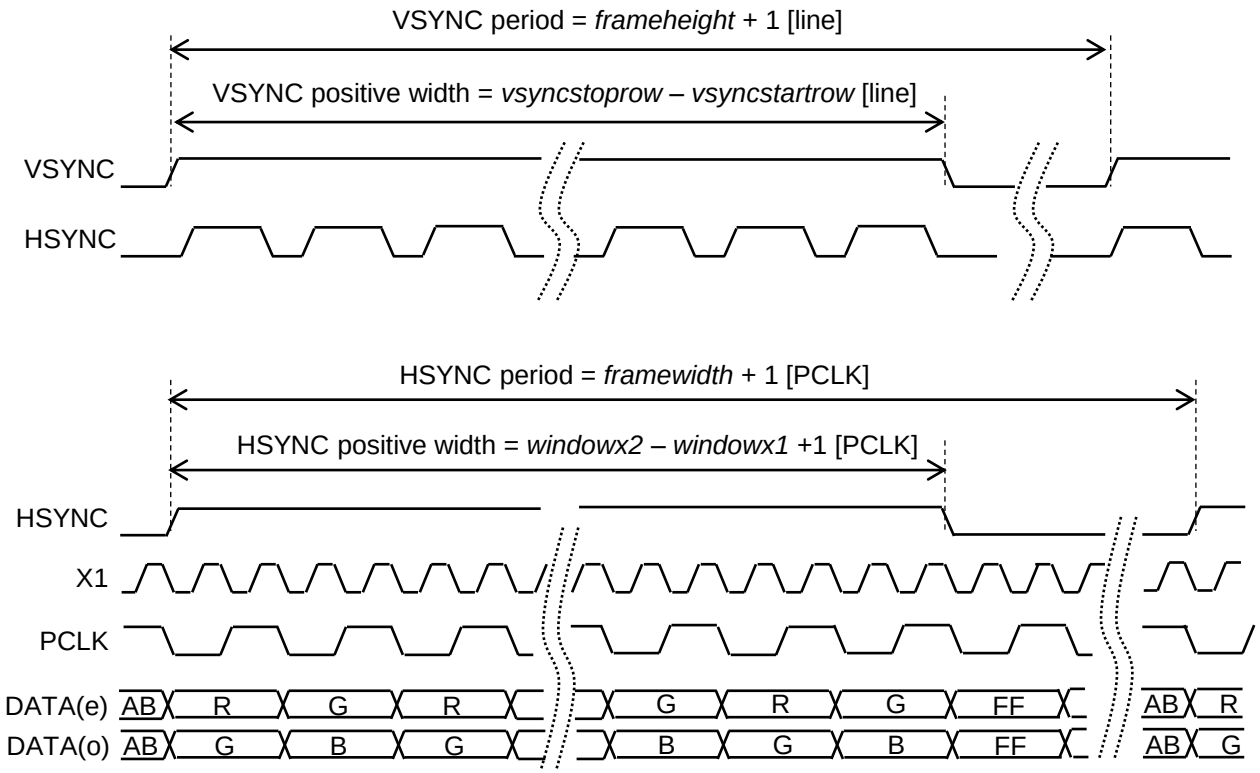
HSYNC positive width = 2 x (*windowx2* - *windowx1* + *1)* [PCLK]

Data sequence of YUV format can change to [U, Y, V, Y], [V, Y, U, Y], [Y, U, Y, V] and [Y, V, Y, U] by *format* (register value). Data value can be selected in Invalid or blanking region.



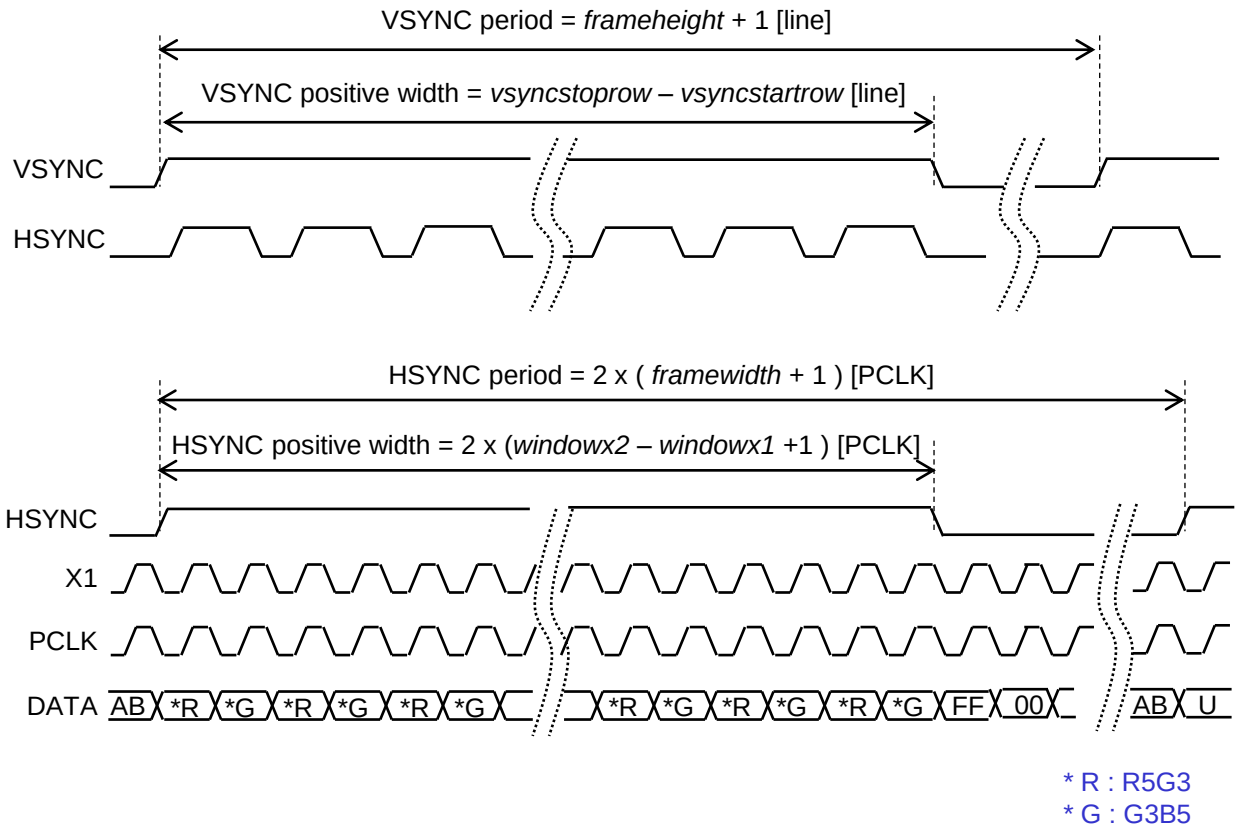
[Fig. 5] Timing Diagram for VSYNC, HSYNC, X1, PCLK and Data (YUV mode : default)

[Fig. 6] shows the bayer data sequence of PC3089N. The default sequence Bayer data is [RGRG…] for even rows and [GBGB…] for odd rows.



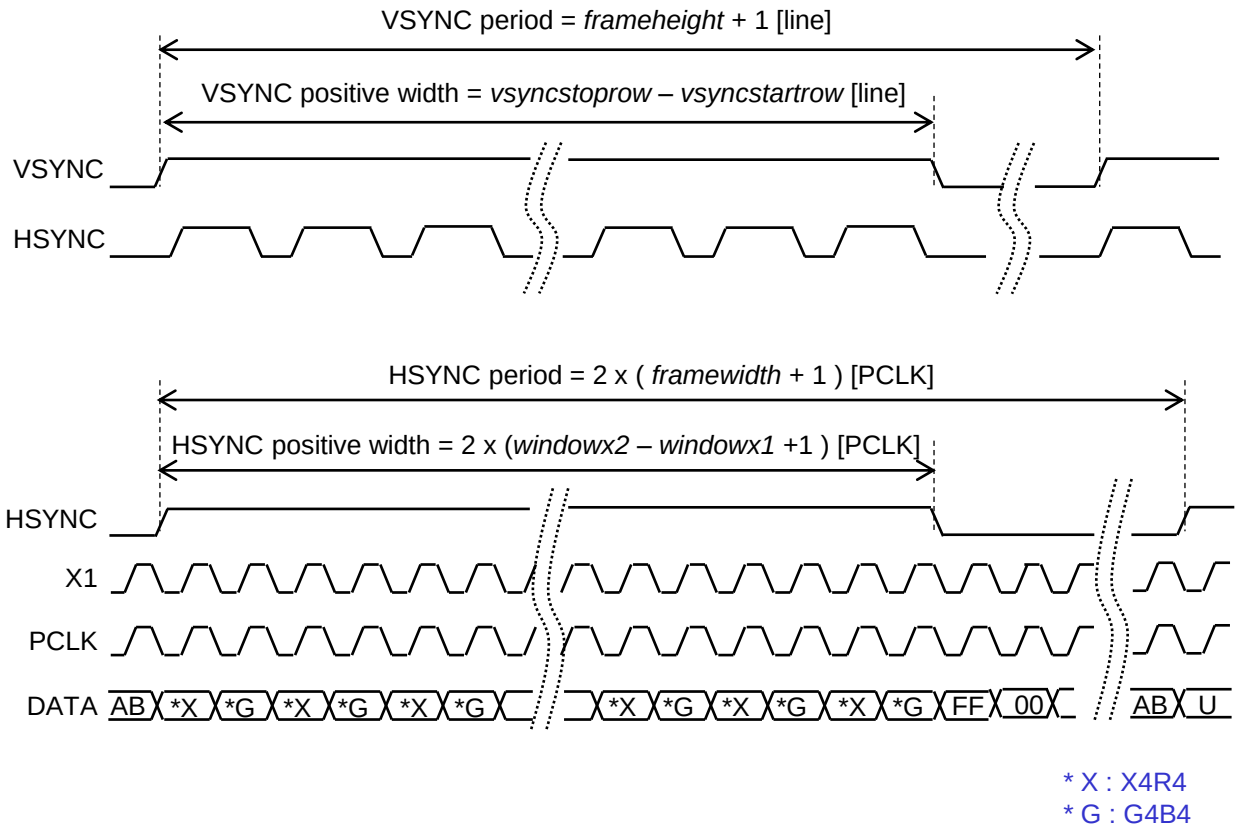
[Fig. 6] Timing Diagram for VSYNC, HSYNC, X1, PCLK and Data (Bayer mode)

[Fig. 7] shows the RGB565 data sequence of PC3089N. The RGB565 data sequence can change to [R5G3, G3R5], [G3R5, R5G3], [B5G3, G3R5] and [G3R5, B5G3] by *format* (register value).



[Fig. 7] Timing Diagram for VSYNC, HSYNC, X1, PCLK and Data (RGB565 mode)

[Fig. 8] shows the RGB444 data sequence of PC3089N. The RGB444 data sequence can change to [x4R4, G4B4] and [G4B4, X4R4] by *format* (register value).

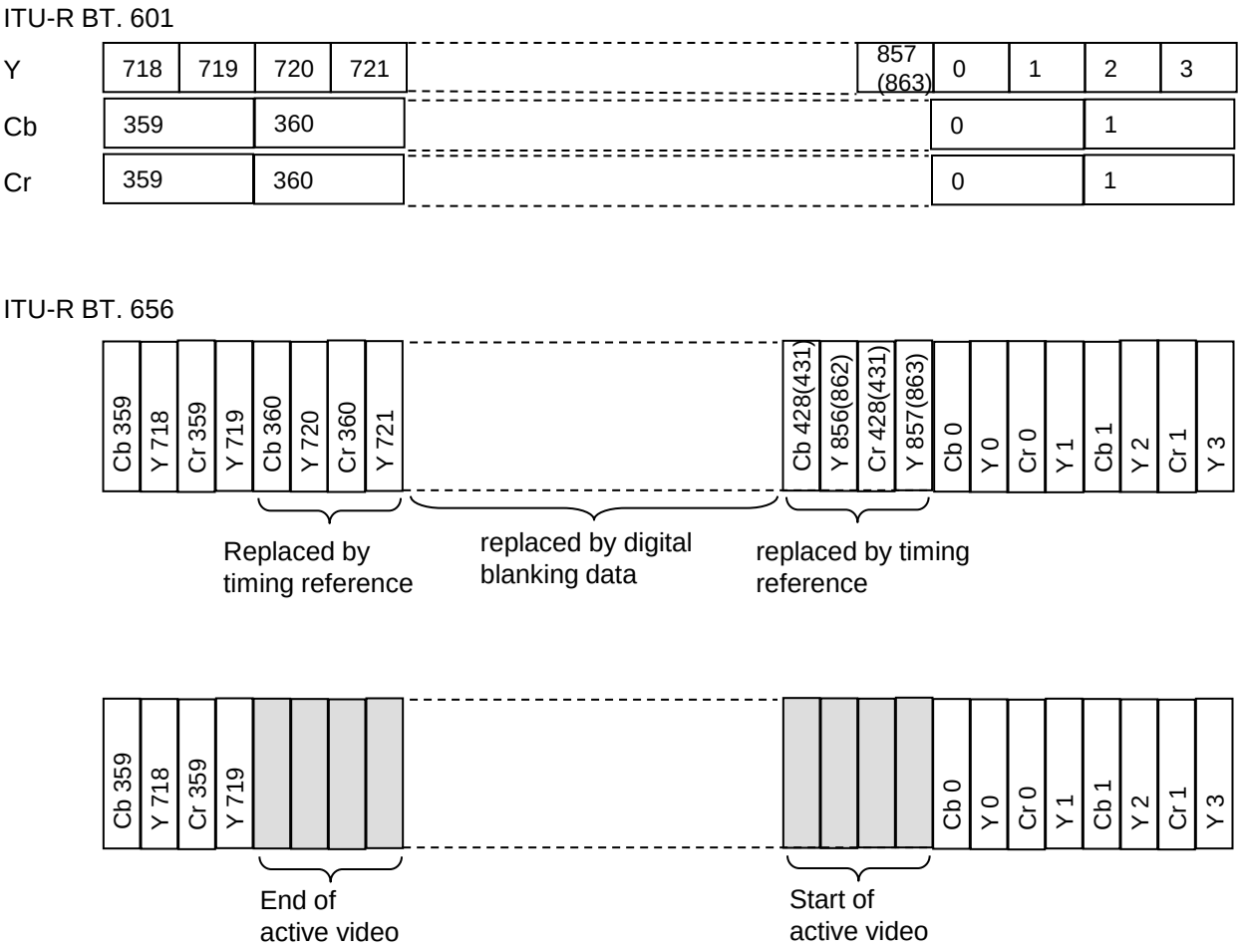


[Fig. 8] Timing Diagram for VSYNC, HSYNC, X1, PCLK and Data (RGB444 mode)

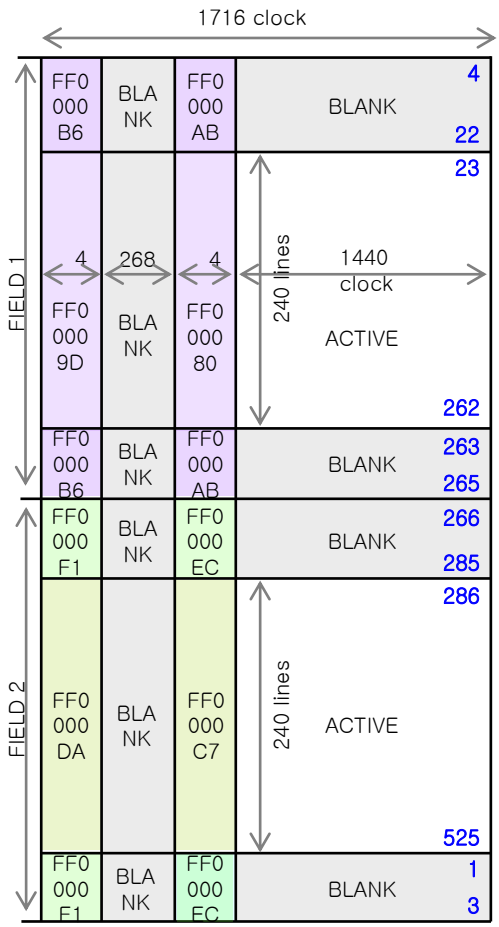
2) ITU-R BT656 (CCIR656)

[Fig. 9] shows ITU-R BT601 and ITU-R BT656 timing diagram. Sampling clocks of ITU-R BT601 and ITU-R BT656 are 13.5MHz and 27MHz respectively. ITU-R BT656 format is generated from ITU-R BT601 format data by serialization and timing reference. Timing reference indicates Start or End of video. It includes field, vsync and hsync information.

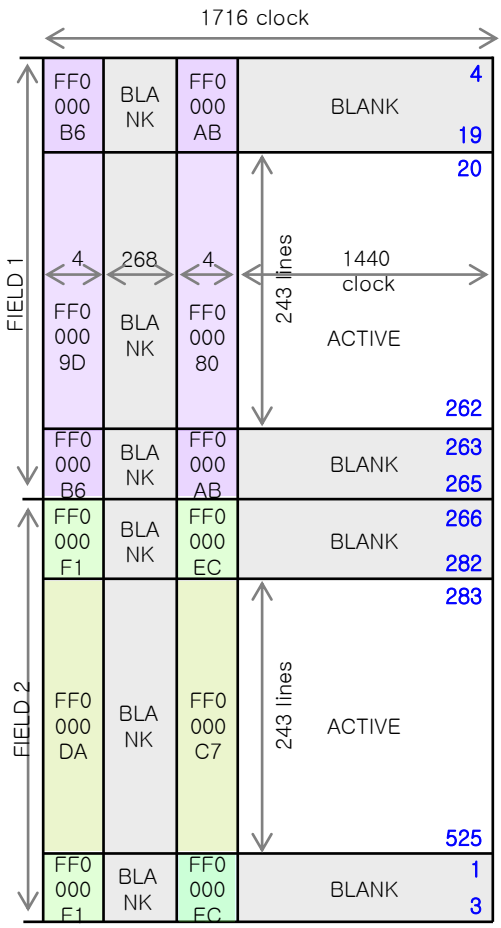
PC3089N provides two kinds of active video sizes with BT656 format such as 720x480i and 720x576i ('i' stands for interlaced scan). The horizontal size is stretched to 720 pixels. 720x480i size BT656 supports for 525-line video, and 720x576i size BT656 for 625-line video. Horizontal timing of 720x480i and 720x576i size BT656 is shown in [Fig. 9] and vertical Timing diagram is shown in [Fig. 10]



[Fig.9] Timing Diagram of ITU-R BT601 and ITU-R BT656



525-line, NTSC ITU-R BT656 Standard like Format (*bt656_sel* = 00b)



525-line, NTSC ITU-R BT656 Standard Format (*bt656_sel* = 10b)

[Fig. 10] Vertical Timing Diagram of ITU-R BT656 (continue)

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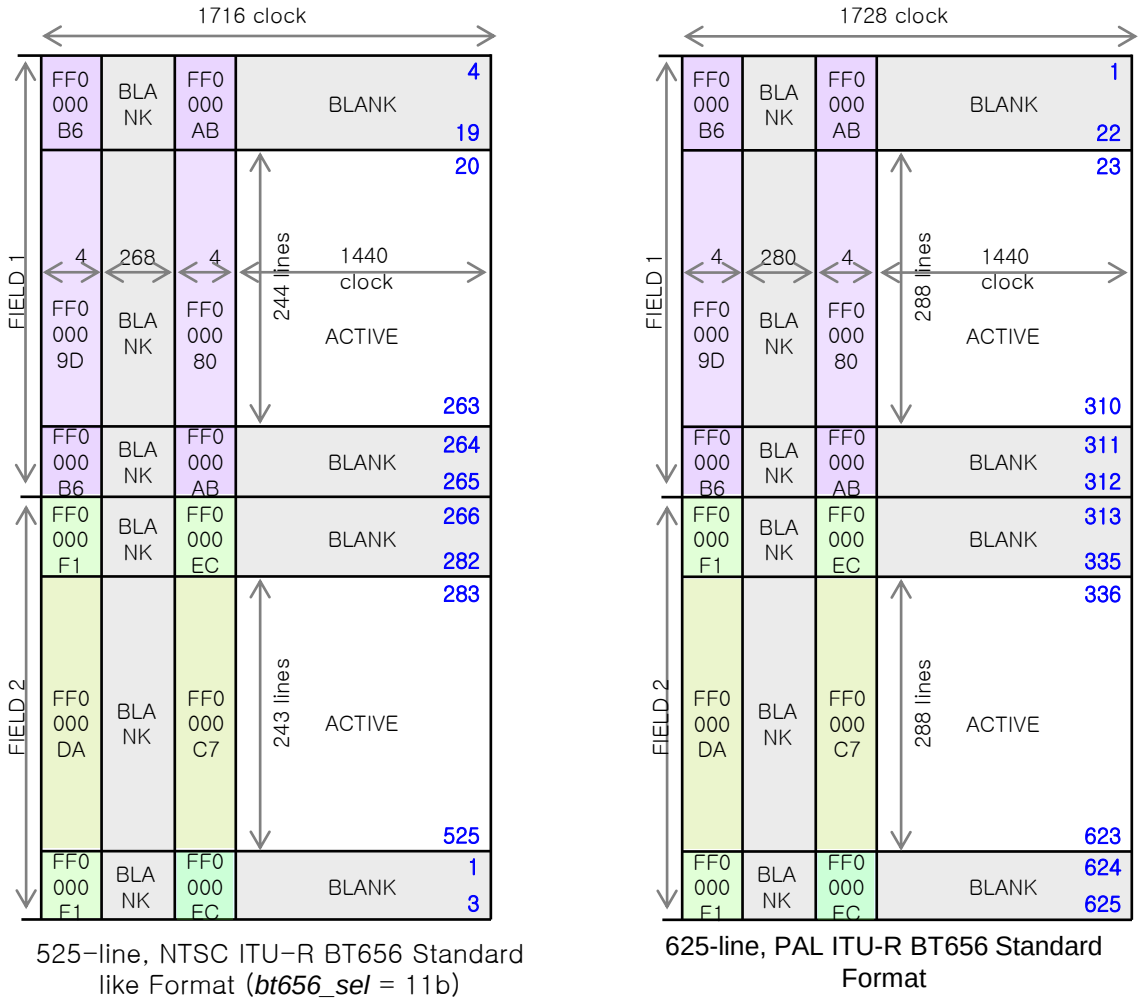
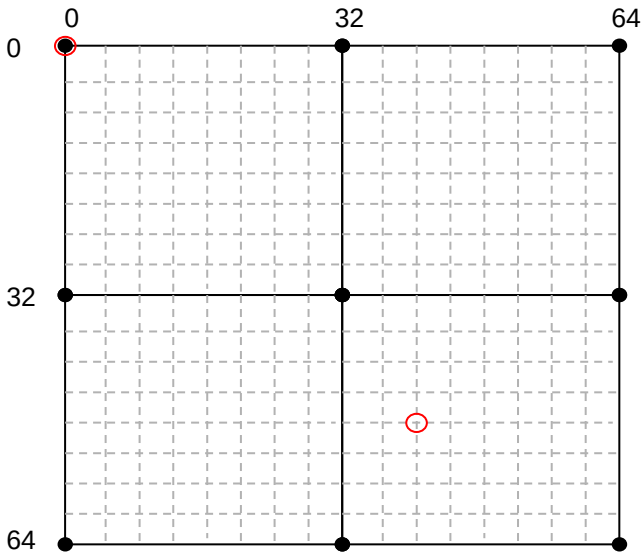


[Fig. 10] Vertical Timing Diagram of ITU-R BT656

- The numbers on the image indicate Line number.
- For 525-line format, active lines are 240, 243 or 244 per a field. For 625-line format, active lines are 288 per a field.
- Vertical Timing is slightly different to Typical BT.656 for 525-line format. In active data regions above [Fig. 10] they have only active pixel data not any fixed data (eg. black data).

▶ Scaling



[Fig. 11] Free Scaling

● Full image pixel locations

X points = 32 * M

Y points = 32 * N

○ Scaled image sampling points

X Sampling points = reg_scale_x * P

Y Sampling points = reg_scale_y * Q

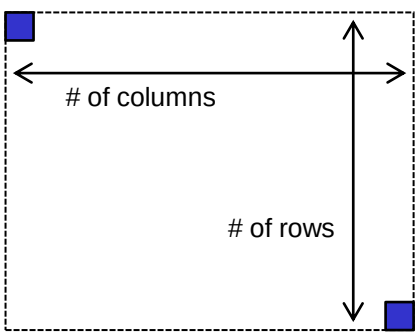
← Example

reg_scale_x = 40

reg_scale_y = 48

(reg_window_x1, reg_window_y1)

minimum = (1, 1)



[Fig. 12] Output Image Size

(reg_window_x2, reg_window_y2)

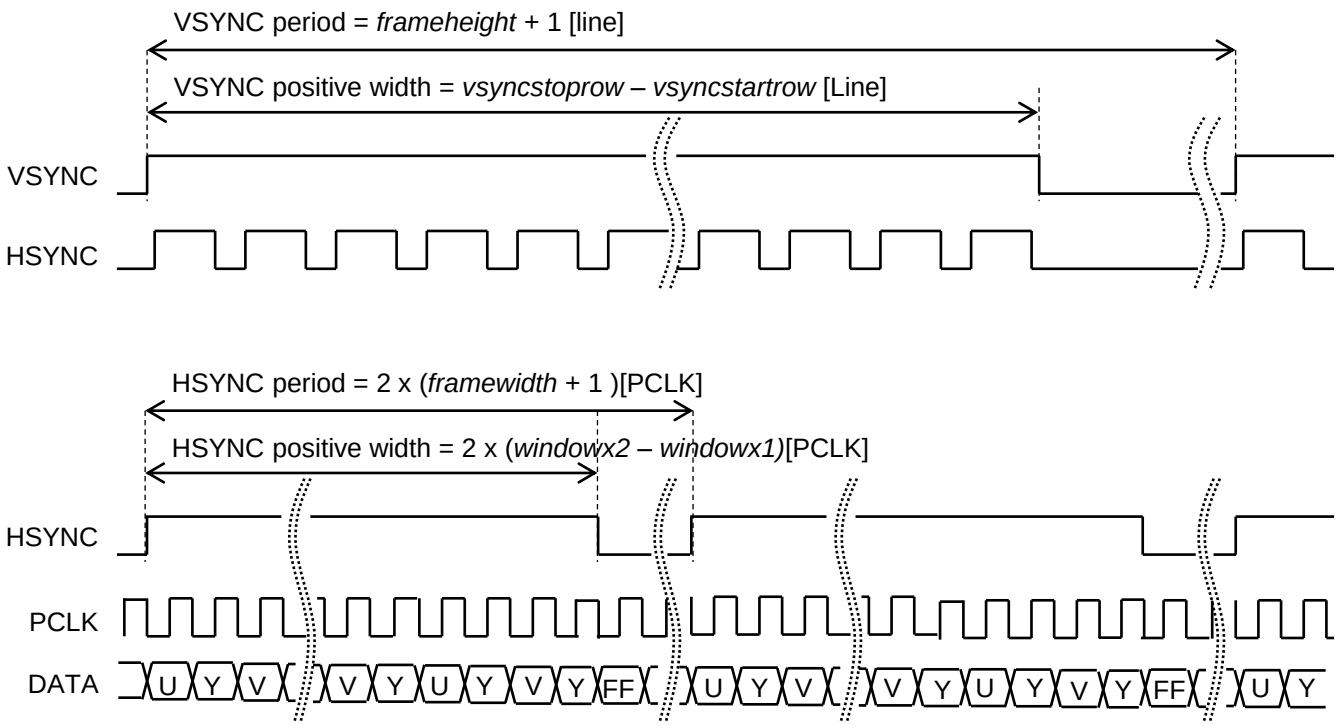
maximum = (960, 480)

Where,

Number of columns = reg_window_x2 - reg_window_x1 + 1

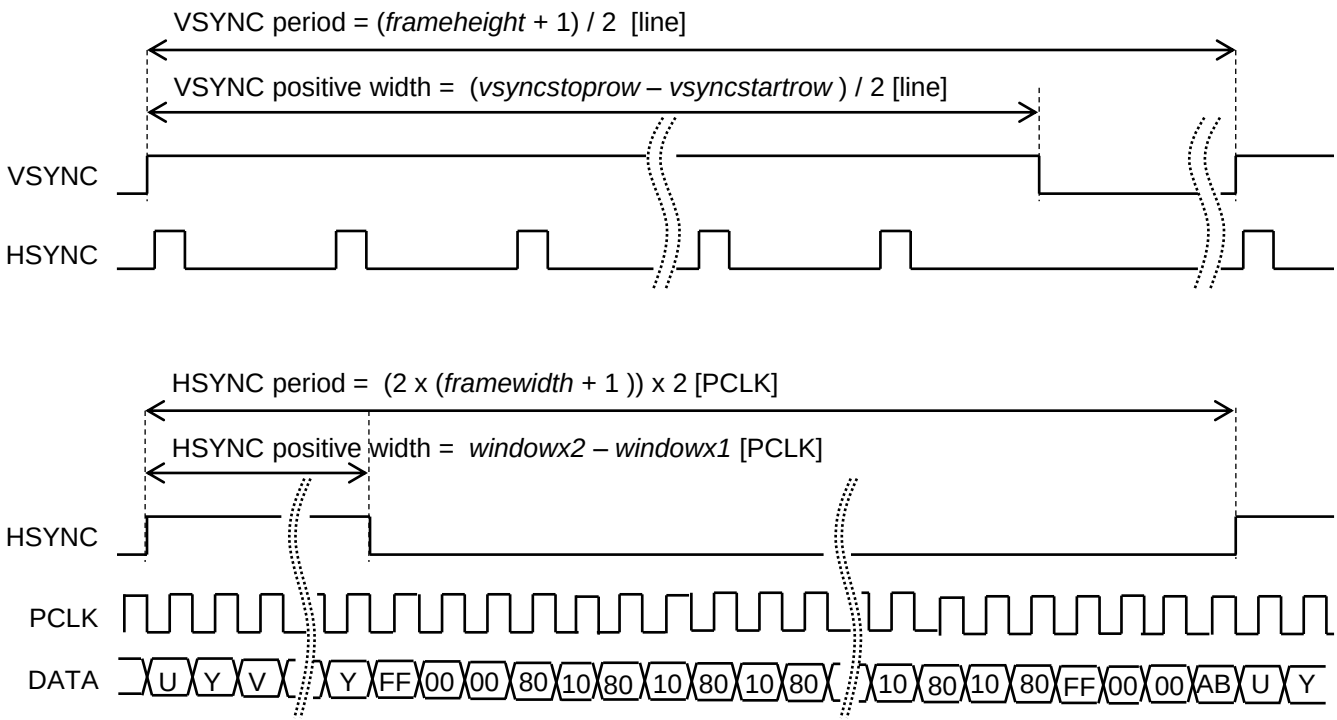
Number of rows = reg_window_y2 - reg_window_y2 + 1

(1) X Full Sampling Mode / Y Full Sampling Mode



[Fig. 13] Timing Diagram for Full Mode

(2) X 1/2 Scale Mode / Y 1/2 Scale Mode



[Fig. 14] Timing Diagram for XY-Scaling Mode

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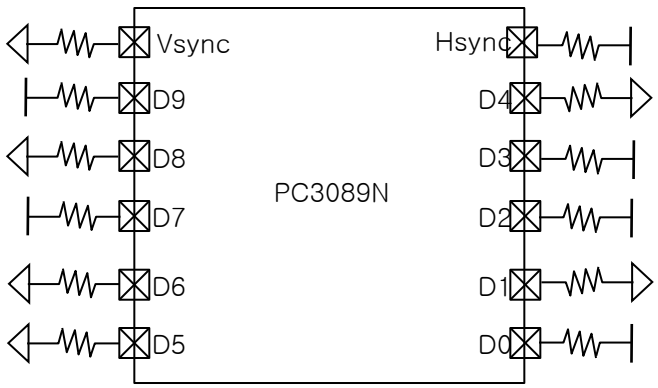
▶ *Wire-strapping*

Wire-strapping is a function of chip mode selection. Chip mode is automatically selected according to D9~D0 pads wired with pull-up or pull-down. [Fig.15] shows an example of Wire-strapping configuration and [Table 2] shows chip mode selection by wire-strapping.



[Fig.15] Example of Wire-strapping

		vsync	hsync	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TV_MODE	(M)NTSC	-	-	-	-	-	-	-	L	L	L	-	-
	NTSC-J	-	-	-	-	-	-	-	L	L	H	-	-
	(M)PAL	-	-	-	-	-	-	-	L	H	L	-	-
	(Nc)PAL	-	-	-	-	-	-	-	L	H	H	-	-
	(B,D,G,H,I) PAL	-	-	-	-	-	-	-	H	L	L	-	-
	(N)PAL	-	-	-	-	-	-	-	H	L	H	-	-
	NTSC-4.43	-	-	-	-	-	-	-	H	H	L	-	-
FLICKER	No Flicker cancel	-	-	-	-	-	L	L	-	-	-	-	-
	Manual-A	-	-	-	-	-	L	H	-	-	-	-	-
	Manual-B	-	-	-	-	-	H	L	-	-	-	-	-
	Auto Flicker cancel	-	-	-	-	-	H	H	-	-	-	-	-
MIRROR	NO MIRROR	-	-									H	L
	MIRROR-V	-	-	-	-	-	-	-	-	-	-	L	L
	MIRROR-H	-	-	-	-	-	-	-	-	-	-	H	H
	MIRROR-VH	-	-	-	-	-	-	-	-	-	-	L	H
BLC(or (general[0])	ON	-	-	-	-	H	-	-	-	-	-	-	-
	OFF	-	-	-	-	L	-	-	-	-	-	-	-
Indoor/ Outdoor (or general[1])	Indoor mode	-	-	-	H	-	-	-	-	-	-	-	-
	Outdoor mode	-	-	-	L	-	-	-	-	-	-	-	-

[Table 2] Wire-strapping (continue)

		vsync	hsync	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OSD	Enable	-	-	H	-	-	-	-	-	-	-	-	-
	Disable	-	-	L	-	-	-	-	-	-	-	-	-
MASTER MODE	ON	H	-	-	-	-	-	-	-	-	-	-	-
	OFF	L	-	-	-	-	-	-	-	-	-	-	-
General[2]	'1'	-	H	-	-	-	-	-	-	-	-	-	-
	'0'	-	L	-	-	-	-	-	-	-	-	-	-

[Table 2] Wire-strapping

When using BLC, Indoor/Outdoor strap as general[1:0] with External ROM, BLC, Indoor/Outdoor setting should be written in External ROM.
In detail, Refer to . ([Table 6], [Table 7])

[Table 3] shows TV_mode wire-strapping registers. These registers are changed by D4~D2.

Register name	"000b" (M)NTSC	"001b" NTSC-J	"010b" (M)PAL	"011b" (Nc)PAL	"100b" (OTHER)PALs	"101b" (N)PAL	"110b" NTSC-4.43
pad_control7	01	01	01	01	01	01	01
chip_mode	00	00	00	01	01	01	00
framewidth_h	03	03	03	04	04	04	03
framewidth_l	59	59	59	0D	0D	0D	59
fd_a_step_h	03	03	03	04	04	04	03
fd_a_step_l	E8	E8	E8	BD	BD	BD	E8
fd_b_step_l	40	40	40	F0	F0	F0	40
fd_period_a_h	01	01	01	00	00	00	01
fd_period_a_m	03	03	03	D8	D8	D8	03
fd_period_a_l	80	80	80	F8	F8	F8	80
fd_period_b_m	3B	3B	3B	01	01	01	3B
fd_period_b_l	0D	0D	0D	00	00	00	0D
fd_period_c_h	06	06	06	05	05	05	06
fd_period_c_m	27	27	27	15	15	15	27
fd_fheight_a_l	0C	0C	0C	07	07	07	0C
fd_fheight_b_l	0C	0C	0C	07	07	07	0C
expfrmH_l	07	07	07	02	02	02	07
midfrmheight_l	07	07	07	02	02	02	07
maxfrmheight_l	07	07	07	02	02	02	07
vsyncstoprow_f0_l	06	06	06	36	36	36	06
vsyncstartrow_f1_l	1E	1E	1E	50	50	50	1E
vsyncstoprow_f1_l	0D	0D	0D	6F	6F	6F	0D
osd_efld_s_h	00	00	00	00	00	00	00
osd_efld_s_l	01	01	01	01	01	01	01
osd_ofld_s_h	01	01	01	01	01	01	01
osd_ofld_s_l	0A	0A	0A	39	39	39	0A
enc_mode	00	00	03	02	01	01	00
enc_blankL	F0	F0	F0	FC	FC	F0	F0
enc_pedestal	2A	00	2A	00	00	2A	2A
enc_burst	80	82	8C	8A	9C	9A	82
enc_Ygain	82	8D	82	89	89	82	82
enc_Ugain	6F	78	6F	75	75	6F	6F
enc_Vgain	9C	A9	9C	A6	A6	9C	9C
enc_Crange_L	48	62	48	5B	5B	48	48
enc_chroma_max_L	CD	DF	CD	D7	D7	CD	CD
enc_chroma_min_L	6D	35	6D	45	45	6D	6D
enc_scfreq	00	00	03	02	01	01	01
hsync_p_toffset	12	12	12	00	00	06	12
burst_duration	00	00	89	89	00	00	8D
l_blank_start	0C	0C	0D	12	15	10	0C
l_blank_stop	02	02	03	0B	0B	00	02
sync_rising	04	04	04	08	08	07	04
burst_toffset	88	88	08	8A	96	96	88
encdat_rising	04	04	04	07	08	07	04
setup_w	07	00	07	00	00	07	07

[Table 3] TV Mode Registers

[Table 4~7] show registers and setting values related with Flicker mode, Mirror mode, BLC mode and Indoor/Outdoor mode.

	"00b"	"01b"	"10b"	"11b"
Register name	Normal(off)	manual A	manual B	auto_fd
flicker_control_1	00	08	04	40

[Table 4] Flicker Mode Register

	"00b"	"01b"	"10b"	"11b"
Register name	V mirror	HV mirror	No mirror	H mirror
mirror	02	03	00	01

[Table 5] Mirror Mode Register

	vsync="0b"	vsync="1b"	vsync="1b"
Register name		BLC off ("0b")	BLC on ("1b")
ae_weight1	08	08	08
ae_weight2	08	08	08
ae_weight3	08	08	08
ae_weight4	08	08	08
ae_weightc	08	08	38
max_yt1	98	98	98
max_yt2	50	50	50
min_yt1	98	98	98
min_yt2	50	50	50

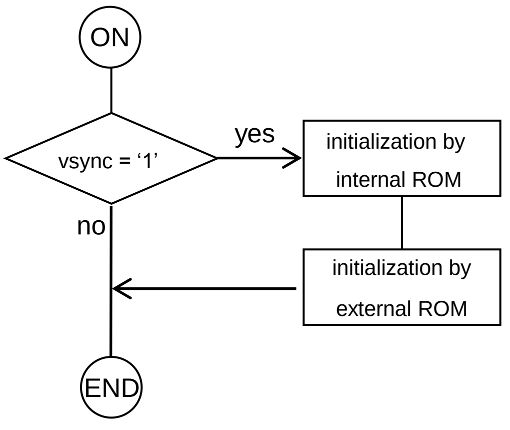
[Table 6] BLC Mode Register

	vsync="0b"	vsync="1b"	vsync="1b"
Register name		Outdoor ("0b")	Indoor ("1b")
awb_rgain_min1	00	64	00
awb_rgain_min2	00	64	00
awb_rgain_max1	FF	90	FF
awb_rgain_max2	FF	90	FF
awb_bgain_min1	00	54	00
awb_bgain_min2	00	54	00
awb_bgain_max1	FF	68	FF
awb_bgain_max2	FF	68	FF

[Table 7] Indoor/Outdoor Mode Register

Caution : If sensor is operated by not master mode (vsync = "0b") BLC, Indoor/Outdoor strap is can't be operated. (adaptive fixed value)

[Table 8] show registers and setting values related with master mode.



[Fig. 16] shows initialization process of registers. When vsync is high, register default values are initialized by internal ROM and external ROM.

▶ If you want to see more processes, see [Fig. 20].

[Fig. 16] Initialization Process of Registers

	vsync = 0b	vsync = 1b
Registers	master mode off	master mode on

	vsync = 0b	vsync = 1b
Registers	master mode off	master mode on

[Table 8] Internal ROM Registers Setting (continue)

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

	vsync = 0b	vsync = 1b
Registers	master mode off	master mode on

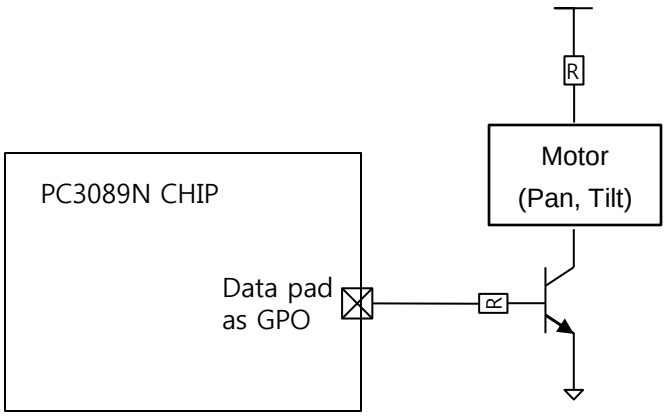
	vsync = 0b	vsync = 1b
Registers	master mode off	master mode on

[Table 8] Internal ROM Registers Setting

▶ Data Pads as GPO

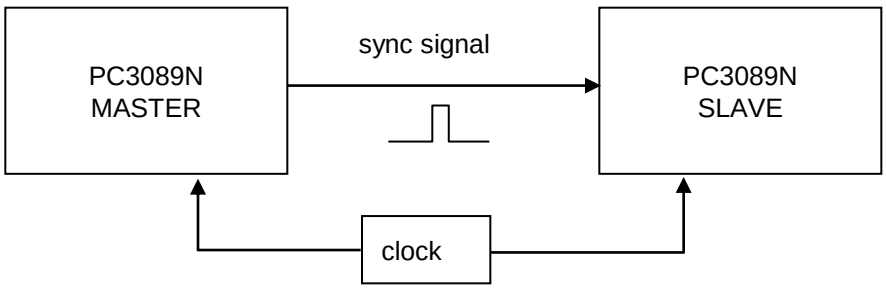
Data pads(D9~D2) can be used as GPO(General Purpose Output) when user doesn't use digital output. If *reg_pad_control3*[0] is set to '1b', user can control data pads outputs manually by setting *reg_pad_control9*.

[Fig. 17] shows an example of using GPO pad. User can control a motor to pan or tilt the sensor module by controlling GPO pad data.



[Fig. 17] Example of Using GPO Pad

▶ Genlock(master/slave) Operation



[Fig. 18] System Configuration for Genlock

Registers	Values	Descriptions
pad_control5(3)	'1b'	Enable GENO pad
bayer_control_01(5)	'1b'	External Sync ON
bayer_control_01(4)	'1b'	External Sync Master
rcount_genlock_h/l, ccount_genlock_h/l	same as slave's	Synchronizing time control between master and slave

[Table 9] Registers Setting for Genlock Master

Registers	Values	Descriptions
pad_control5(0)	'1b'	Enable GENI pad
bayer_control_01(5)	'1b'	External Sync ON
bayer_control_01(4)	'0b'	External Sync Slave
rcount_genlock_h/l, ccount_genlock_h/l	same as master's	Synchronizing time control between master and slave

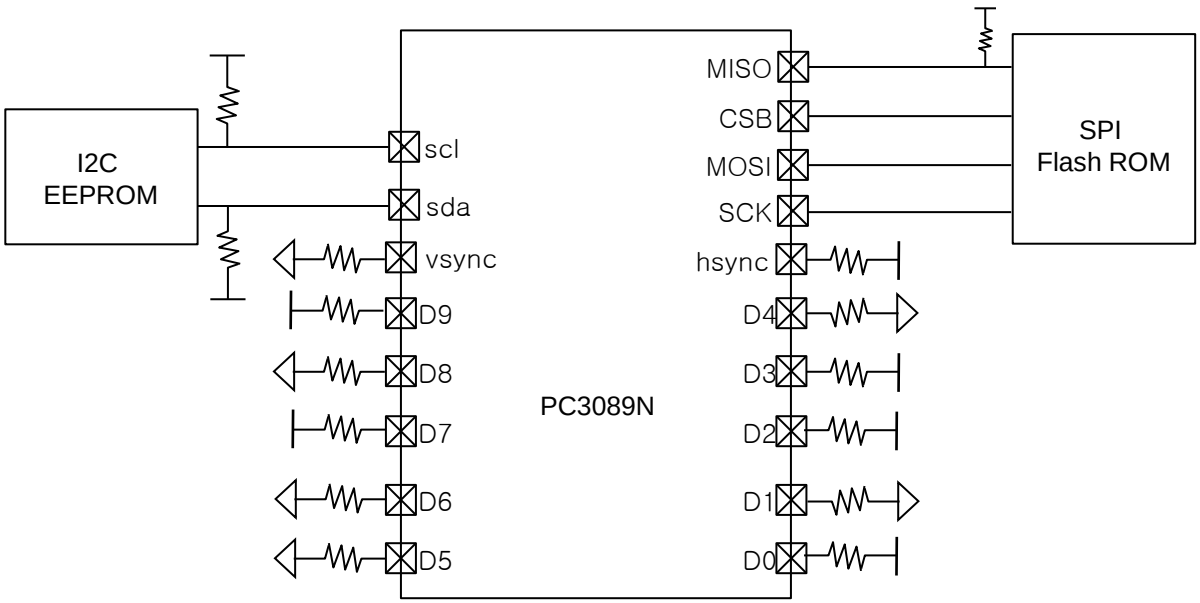
[Table 10] Registers Setting for Genlock Slave

Genlock is a function to synchronize digital output data of two or more PC3089Ns. One of the PC3089N must be a master and others are slaves. The master generates genlock signal by the *rcount_genlock_h/l* and *ccount_genlock_h/l*. Then slaves receive the genlock signal from the master and set their counters with the *rcount_genlock_h/l* and *ccount_genlock_h/l*.

Caution : When user want to use one SCL/SDA line with several PC3089Ns, user must connect CADDR1 and CADDR0 pads to pull-up or pull-down.

▶ Registers Initializing

PC3089N supports user tuning registers can be set by I2C EEPROM or SPI Flash ROM initially. [Fig. 19] shows how to connect PC3089N with external ROM(I2C EEPROM/SPI Flash ROM). After reset, PC3089N reads initialization table stored in external ROM. [Fig. 20] shows Initialization routine.



[Fig. 19] Example of Connection with External ROM

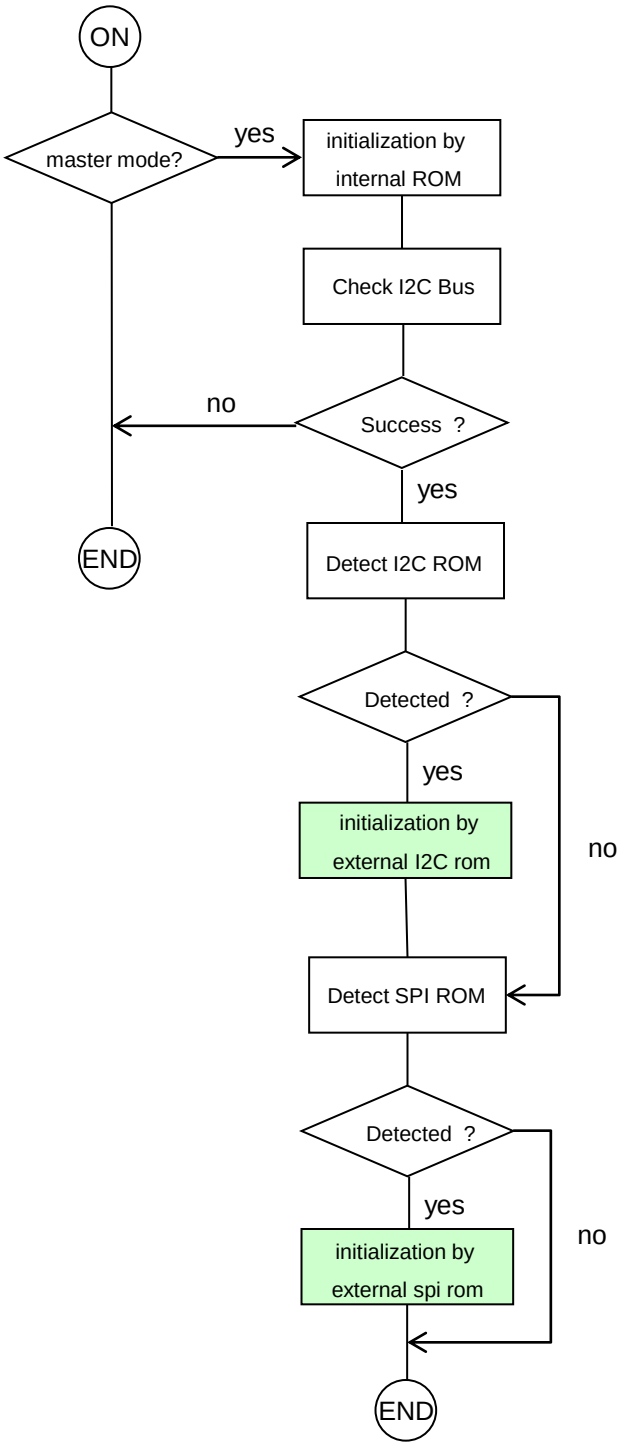
Initialization process is as below.

Case1 : Connect with I2C EEPROM & disconnect with SPI Flash ROM :
PC3089N is initialized by I2C EEPROM. SPI Flash ROM process is skipped.

Case2 : Connect with SPI Flash ROM & disconnect with I2C EEPROM :
PC3089N is initialized by SPI Flash ROM. I2C EEPROM process is skipped.

Case3 : Connect with I2C EEPROM & connect with SPI ROM :
PC3089N registers are overwritten by SPI Flash ROM.

* Caution : It covers up to 2K bytes I2C EEPROM. If the I2C EEPROM size is more than 2K bytes then register setting does not operate.



[Fig. 20] Initialization Routine

▶ Access Time of External I2C Master

Because I2C master was designed as a single master and shares SDA/SCL with I2C slave, external I2C master must access to PC3089N after initialization routine as [Fig. 20]. Initialization time depends on the number of registers to be written by external I2C rom. If the number of setting register is 1024d (max.), it will take initialization time about 140ms to be finished after reset. After that, an external I2C master should access to PC3089N.

Access time as below.

Case1 : master enable and with external I2C rom : variable (depend on register numbers, max. 140ms)

Case2 : master enable and without external I2C rom : after about 7.1ms(I2C rom detection time)

Case3 : master disable: always possible

▶ ROM Data Structure for Initialization (I2C/SPI ROM)

Address	Contents
0	ABh (Constant) (1)
1	CDh (Constant) (2)
2	reserved(3)
3	reserved(4)
4	reserved(5)
5	reserved(6)
6~8	Common Segment Start
9~11	Common Segment Stop
12~14	TV_mode Segment Start
15~17	TV_mode Segment Stop
18~20	Mirror Segment Start
21~23	Mirror Segment Stop
24~26	Flicker Segment Start
27~29	Flicker Segment Stop
30~32	General Segment Start
33~35	General Segment Stop
36~38	LED Segment Start(7)
39~41	LED Segment Stop(7)

Address	Contents
…	…
Common Start Common Stop	Common Segment
TVmode Start	NTSC
TVmode Stop	PAL
Mirror Start	Mirror=00
	Mirror=01
	Mirror=10
Mirror Stop	Mirror=11
Flicker Start	Flicker=00
	Flicker=01
	Flicker=10
Flicker Stop	Flicker=11
General start	General=000
	General=001
	. . .
General stop	General=111
LED start	LED on-NTSC
	LED on-PAL
	LED off-NTSC
LED stop	LED off-PAL

[Fig. 21] ROM Data Structure

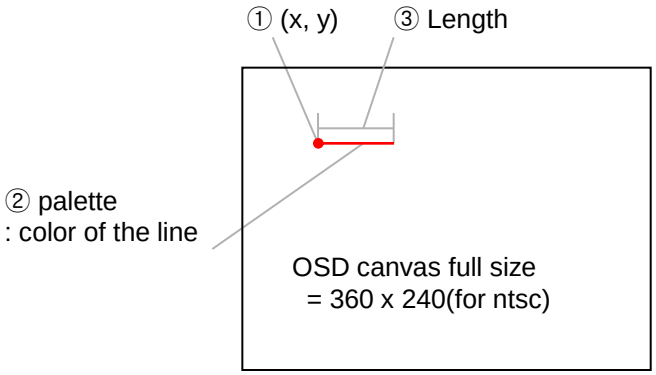
Addresses from 0 to 29d are reserved for Segment Descriptor block. I2C EEPROM and SPI Flash ROM data structure for initialization are same.

(1) ~ (2) : ABCDh in address 0-1 are required to detect external ROM.
(3) ~ (5) : These data are not used, but it should be filled with some data. (caution)
(7) : These are not controlled by strap. If exrom_set_en='1'(led_control2[0]), these segments are applied on next field start after led on/off rising or falling.

If some Segment Start address is greater than Segment Stop address, initialization by the segment will be skipped. (User should be set start address < stop address)

▶ OSD Data Structure

OSD data consists of commands that positions and lines. ***sel_osd_hresol='0' (Reg.A-A2h[4])***



[Fig.22] OSD Data Structure

One line needs 3 components:
position(x, y), palette, length.

1. Position : (x,y) on OSD canvas
➔(2x,2y) on displayed image

2. Palette: represents Y/Cb/Cr information for line.

3. Length: 1 length on OSD canvas
➔ 2 pixels on displayed image

Commands of OSD

1. set_abs_y() : "1 1 0 1 0 ya y9 y8 y7 y6 y5 y4 y3 y2 y1 y0" : set y position = y<10:0>
2. set_rel_y() : "1 1 0 0 0 b2 b1 b0" : y = y + b<2:0>+1
3. set_abs_x() : "1 1 0 1 1 x9 x8 x7 x6 x5 x4 x3 x2 x1 x0 0" : set x position = x<9:0>
4. drw_sline() : "1 0 0 b4 b3 b2 b1 b0" : draw a line of length b<4:0>+1
5. draw_line_a() : "1 1 1 0 0 p2 p1 p0 b7 b6 b5 b4 b3 b2 b1 b0" : draw a line of length b<7:0>+1 using palette<2:0>

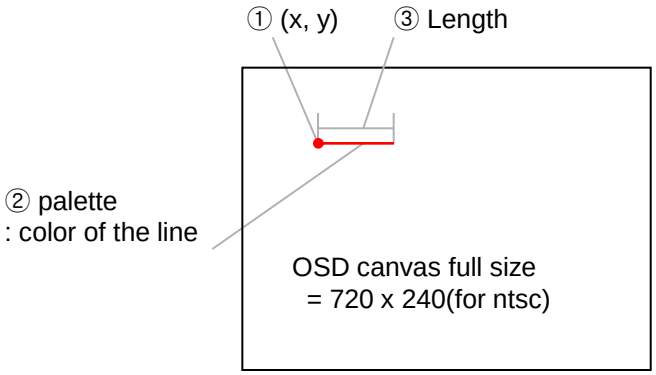
…

OSD data should be stored in SPI Flash ROM. If user want to change displayed OSD images, user should change *spi_saddr*0/1/2/3, *spi_paddr0/1/2/3, spi_addr_update.* For more information, please see the register part.

* Caution : 1. OSD length should be greater than 1.
2. X position should be greater than 0.

▶ *OSD Data Structure*

OSD data consists of commands that positions and lines. ***sel_osd_hresol='1' (Reg.A-A2h[4])***



[Fig.22] OSD Data Structure

One line needs 3 components:
position(x, y), palette, length.

1. Position : (x,y) on OSD canvas
➔(2x,2y) on displayed image

2. Palette: represents Y/Cb/Cr information for line.

3. Length: 1 length on OSD canvas
➔ 2 pixels on displayed image

Commands of OSD

1. set_abs_y() : "1 1 0 1 0 ya y9 y8 y7 y6 y5 y4 y3 y2 y1 y0" : set y position = y<10:0>
2. set_rel_y() : "1 1 0 0 0 b2 b1 b0" : y = y + b<2:0>+1
3. set_abs_x() : "1 1 0 1 1 xa x9 x8 x7 x6 x5 x4 x3 x2 x1 x0" : set x position = x<10:0>
4. drw_sline() : "1 0 0 b4 b3 b2 b1 b0" : draw a line of length b<4:0>+1
5. draw_line_a() : "1 1 1 0 0 p2 p1 p0 b6 b6 b5 b4 b3 b2 b1 b0" : draw a line of length b<6:0>+1 using palette<2:0>

…

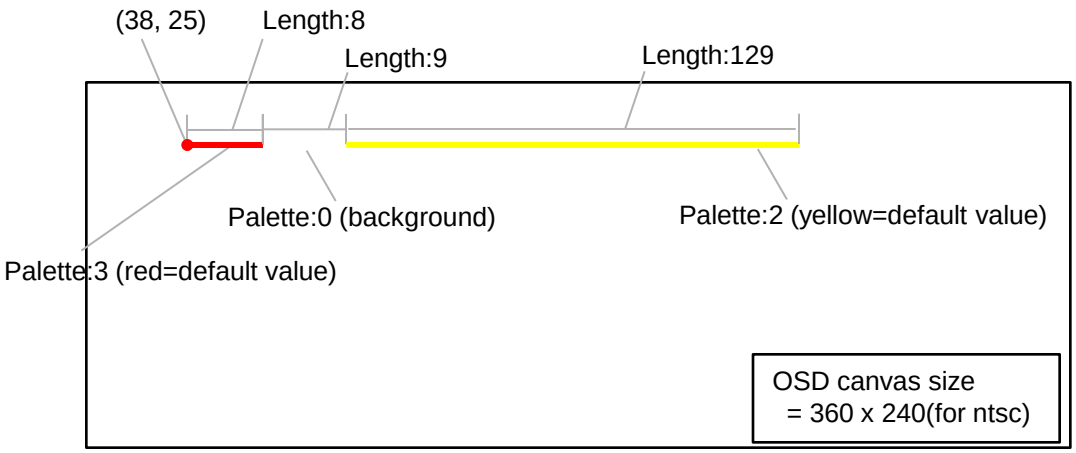
OSD data should be stored in SPI Flash ROM. If user want to change displayed OSD images, user should change *spi_saddr*0/1/2/3, *spi_paddr0/1/2/3, spi_addr_update.* For more information, please see the register part.

* Caution : 1. X position should be greater than 0.

[Fig, 23] shows the example of drawing OSD line.

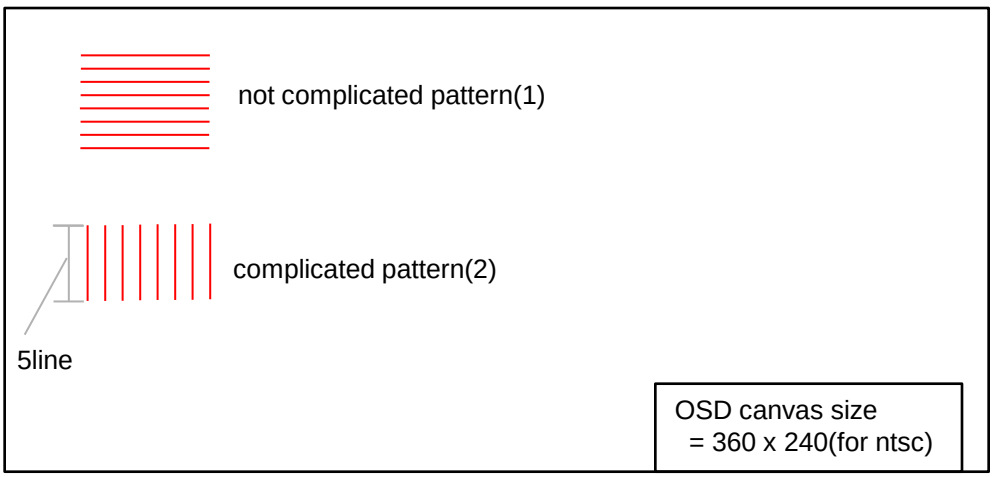
```
SPI ROM OSD data Example

0000h  :  11010000    →  y = 25d
0001h  :  00010001
0002h  :  11000111
0003h  :  11011000    →  x = 38d
0004h  :  01001100
0005h  :  11001110    → draw a line with palette=110, length=8d
0006h  :  10000111
0007h  :  11001000    → skip length9 (palette=000, length=9d)
0008h  :  10001000       palette 0 represents background of image(sensor data).
0009h  :  11100010    → draw a line with palette=010, length=129d
000Ah  :  10000000
```



[Fig.23] Example of Drawing OSD Line

In PC3089N, there is limited to give to expression complex pattern by SPI serial interface because display to read in real time
The criteria is shown at the case of (2) on [Fig, 23]. The amount of OSD data of (2) is around 20 times larger than case (1).

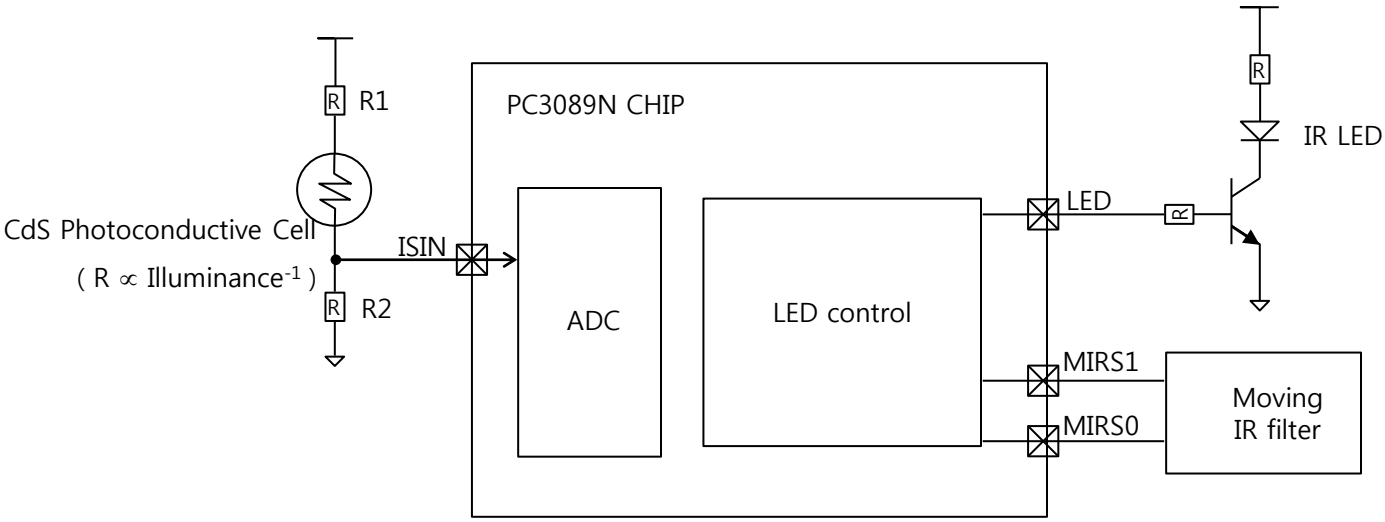


[Fig. 24] Example of Complicated OSD Pattern

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ IR LED & Moving IR filter

The human eyes can only see visible light between 380~770[nm] wavelength. The image sensors can detect wider wavelength than people. Therefore, the sensors can detect the infra-red light but people can not. As a result, when the sensors detect infra-red light, different colors from the real images come out. To prevent this phenomena, camera use the IR-cut filter.



[Fig. 25] IR LED & Moving IR Filter Structure

IR_LED can be controlled by PC3089N which uses analog data from CdS as shown in [Fig. 25]. PC3089N uses IR-cut filter in normal state to prevent above phenomena, but in the dark state, because IR-LED is ON to increase brightness, IR-cut filter should not be used. IR-LED and IR filter can be controlled automatically by PC3089N without changing registers. This means that additional MICOM (MCU) does not need for the IR-LED and IR filter control. As a result, LED and IR filter can be controlled in exact time.

▶ 2-wire Serial Interface Description

The registers of PC3089N are written and read through the 2-wire Serial Interface. The PC3089N has 2-wire Serial Interface slave. The PC3089N is controlled by the Register Access Clock (SCL), which is driven by the 2-wire Serial Interface master. Data is transferred into and out of the PC3089N through the Register Access Data (SDA) line. The SCL and SDA lines are pulled up to VDD by a 2kΩ off-chip resistor. Either the slave or master device can pull the lines down. The 2-wire Serial Interface protocol determines which device is allowed to pull the two lines down at any given time.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a 2-wire Serial Interface device consists of 7-bit of address and 1-bit of direction. A '0' in the LSB of the address indicates write mode, and a '1' indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The SCL pulse is provided by the master. The data must be stable during the HIGH period of the SCL. SDA can be only changed when the SCL is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

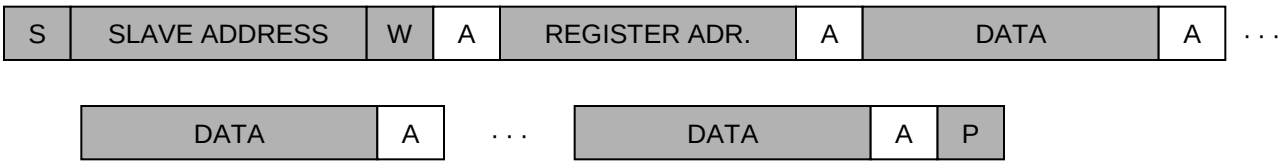
Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a write and a '1' indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master. If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The PC3089N uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit. A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

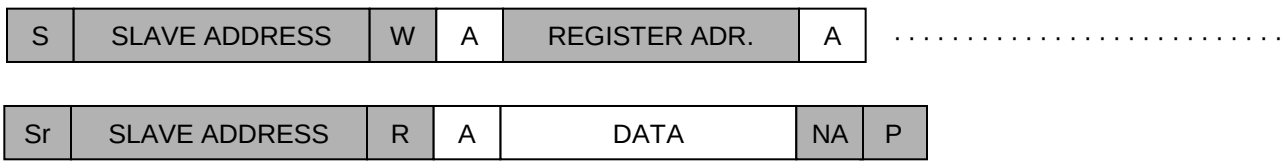
▶ 2-wire Serial Interface Functional Description

Single Write Mode operation

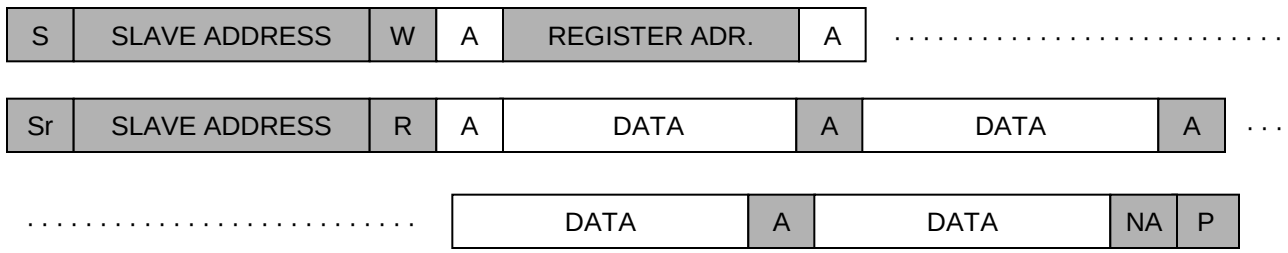
Multiple Write Mode (Register address is increased automatically)[1] operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically)[1] operation



From master to slave From slave to master

S: Start condition. Sr : Repeated Start (Start without preceding stop.)

SLAVE ADDRESS: It can be extended 60h to 67h by CADDR0 and CADDR1 pad

write address	**60h**	**62h**	**64h**	**66h(default)**
read address	**61h**	**63h**	**65h**	**67h(default)**

R/W: Read/Write selection. High = read / LOW = write.

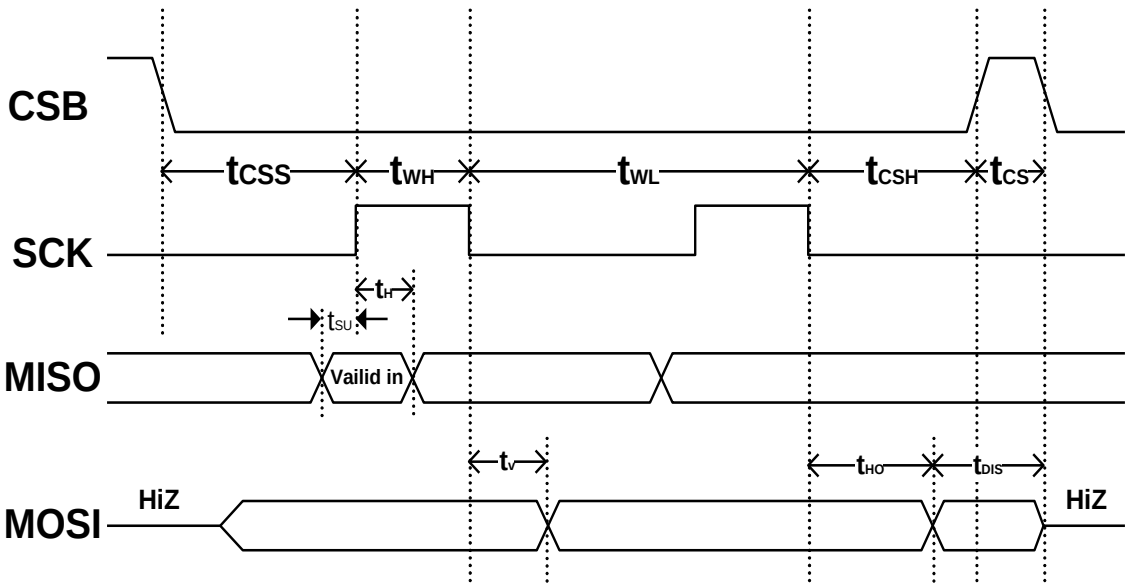
A: Acknowledge bit. NA : No Acknowledge. DATA: 8-bit data. P: Stop condition.

Note 1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

▶ SPI Communication

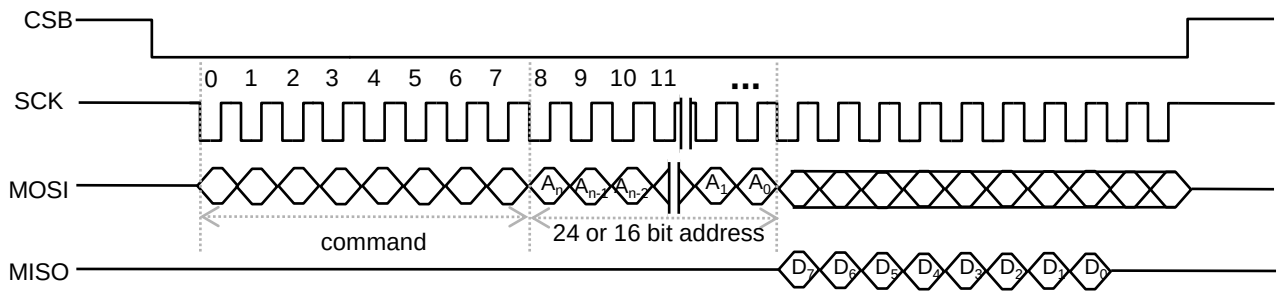
SPI Timing specification

symbol	parameter	min	typ	max	unit
Twh	SCK high time	1/2	1/2		SPI clock
Twl	SCK low time	1/2	1/2		SPI clock
Tcs	CS high time	7	7		SPI clock
Tcss	CS setup time	3/2	3/2		SPI clock
Tcsh	CS hold time	1	1		SPI clock
Tsu	Data in setup time				ns
Th	Data in hold time				ns
Tv	Output valid			1	ppclk
Tho	Output hold time	1/2			ppclk
tdis	Output disable time			0	ns

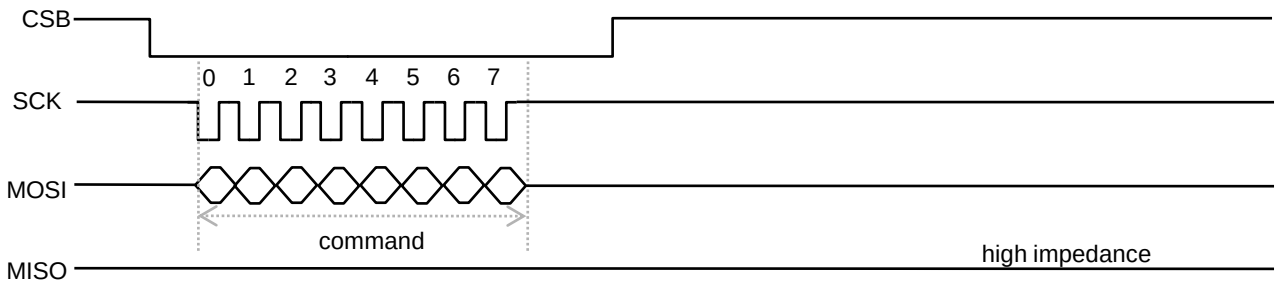


▶ SPI Communication

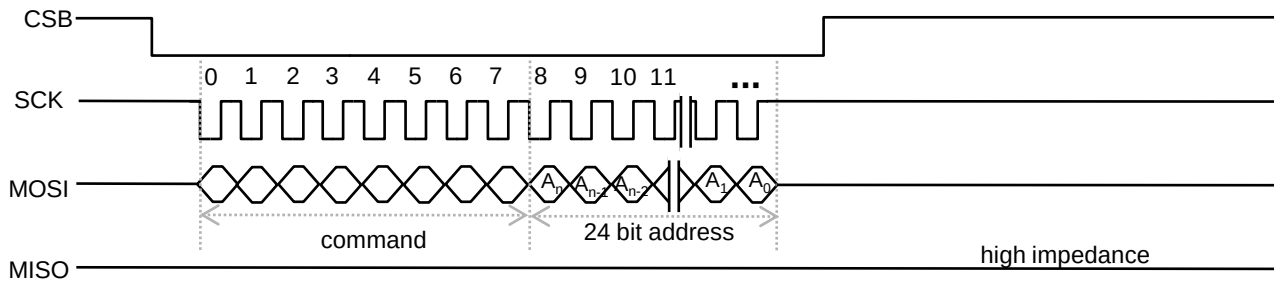
SPI READ command timing



SPI WRITE ENABLE command timing



SPI SECTOR ERASE command timing

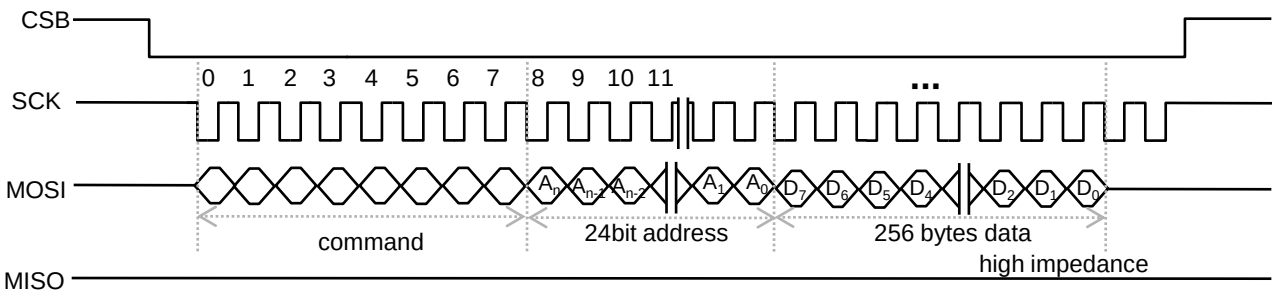


•Caution :

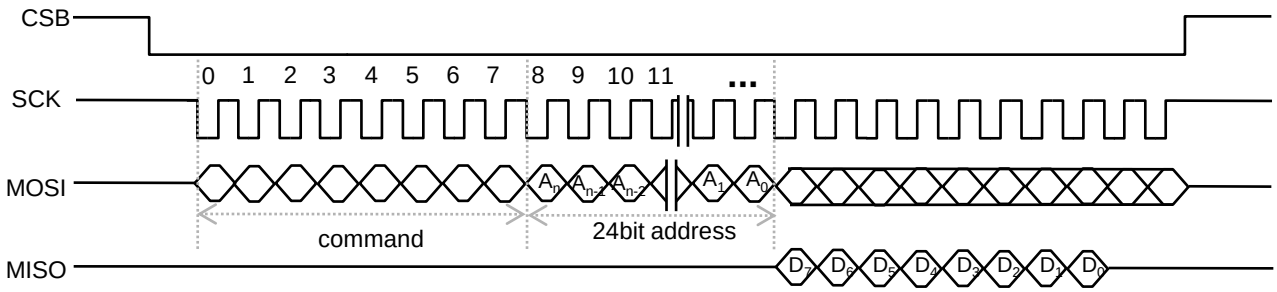
→ It should be use 24bit address SPI ROM for a Embedded OSD control, OSD pointer mode function.

▶ SPI Communication

SPI PAGE PROGRAM command timing



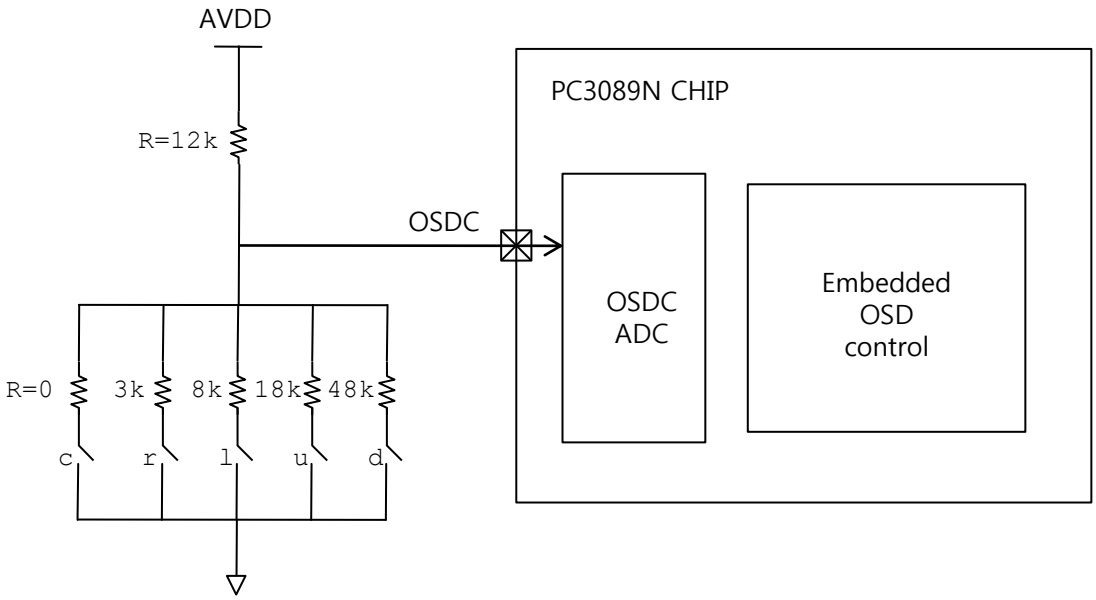
SPI READ STATUS REGISTER command timing



•Caution :

→ It should be use 24bit address SPI ROM for a Embedded OSD control, OSD pointer mode function.

▶ OSDC PAD for Embedded OSD control



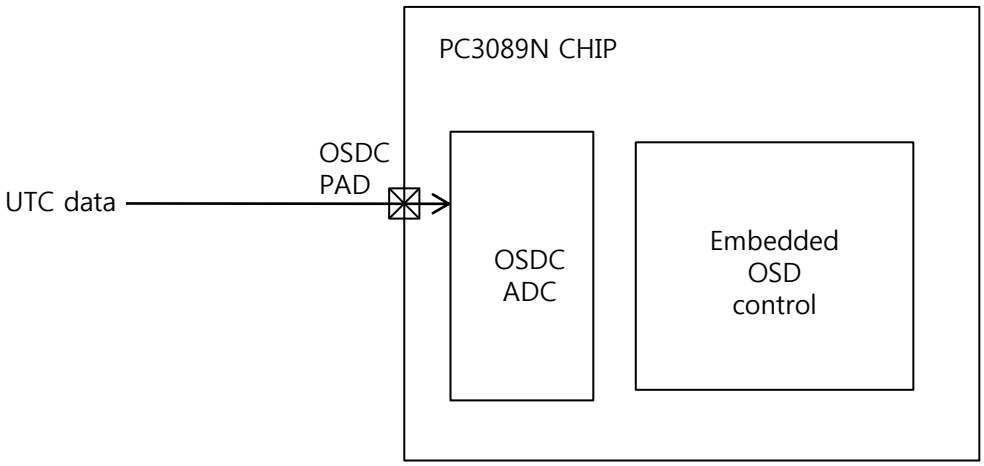
[Fig. 26] Example of Connection with OSDC PAD when using normal switch

The resistance value is just a example at the [Fig.26].

OSDC input voltage(default setting):
- press center(c): 0*AVDD
- press right(r) : 1/5*AVDD
- press left(l) : 2/5*AVDD
- press up(u) : 3/5*AVDD
- press down(d) : 4/5*AVDD
- press none : 1*AVDD

* Voltage error < ±0.05AVDD
* Each key voltage sequence: It can be changed to *sw_comp1~5 (Reg.F-C2h ~ F-CBh)*

▶ OSDC PAD for Embedded OSD control



[Fig. 27] Example of Connection with OSDC PAD when using UTC data

Using OSDC PAD, PC3089N is receive UTC data.

If user use UTC data, sw_control1[4], sw_control2[1] *(Reg.F-A0h ~ F-A1h)* register should be set '1'

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Recommended Power-On/Off sequence

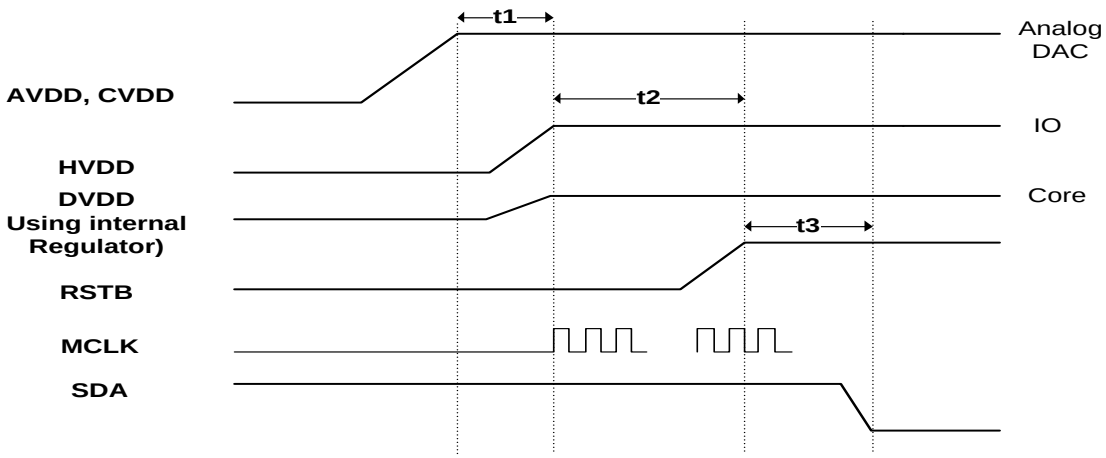
Symbol	Descriptions	Min	Typ	Max	Unit	Remark
t1	From AVDD,CVDD rising to HVDD rising	0			ns	
t2	Sensor reset time	8*mclk				
t3(*)	Initialize time after releasing Reset : Reading internal or external ROM out	8.0(0)		280(0)	ms	Depend on the number of registers
t4	From AVDD,CVDD falling to HVDD falling	0			ns	

•t3 is just applied to strap_master(VSYNC)='1

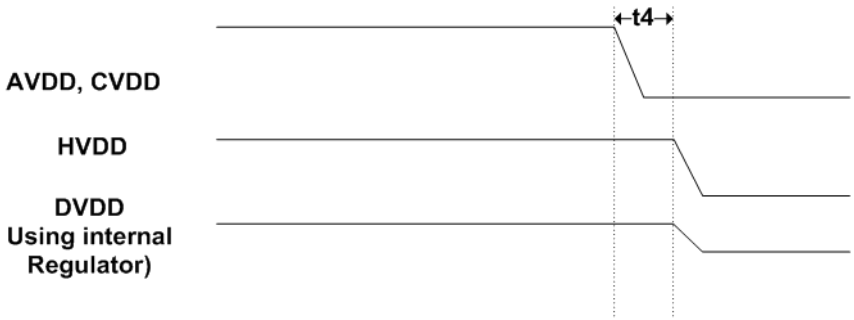
•If user use a strap_master(VSYNC)='0', at that time t3 is 0ms.

[Table 11] Recommended Power-On/Off sequence

※ Power-On Sequence



※ Power-down Sequence



1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Register Tables – Group A

GROUP A									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
0	00	DeviceID_H	48	30	00110000	RO	0	0	device ID
1	01	DeviceID_L	137	89	10001001	RO	0	0	
2	02	RevNumber	0	00	00000000	RO	0	0	revision number
3	03	bank	0	00	xxxx0000	RW	5	0	Register group selector
4	04	chip_mode	u	u	uuuuuuuu	RW	7	aev	chip mode selection(NTSC, PAL, VGA)
5	05	mirror	u	u	uuuuuuuu	RW	7	aev	Mirror
6	06	framewidth_h	u	u	uuuuuuuu	RW	7	aev	Framewidth
7	07	framewidth_l	u	u	uuuuuuuu	RW	7	aev	
8	08	fd_fheight_a_h	2	02	xxx00010	RW	6	aev	Frameheight
9	09	fd_fheight_a_l	u	u	uuuuuuuu	RW	7	aev	
10	0A	fd_fheight_b_h	2	02	xxx00010	RW	6	aev	
11	0B	fd_fheight_b_l	u	u	uuuuuuuu	RW	7	aev	
12	0C	windowx1_h	0	00	xxxxxx00	RW	6	aev	Window
13	0D	windowx1_l	1	01	00000001	RW	6	aev	
14	0E	windowy1_h	0	00	xxxxxx00	RW	6	aev	
15	0F	windowy1_l	1	01	00000001	RW	6	aev	
16	10	windowx2_h	2	02	xxxxxx10	RW	6	aev	
17	11	windowx2_l	208	D0	11010000	RW	6	aev	
18	12	windowy2_h	1	01	xxxxxx01	RW	6	aev	
19	13	windowy2_l	224	E0	11100000	RW	6	aev	
20	14	vsyncstartrow_f0_h	0	00	xxx00000	RW	6	aev	Vsync generation
21	15	vsyncstartrow_f0_l	23	17	00010111	RW	6	aev	
22	16	vsyncstoprow_f0_h	1	01	xxx00001	RW	6	aev	
23	17	vsyncstoprow_f0_l	u	u	uuuuuuuu	RW	7	aev	
24	18	vsyncstartrow_f1_h	1	01	xxx00001	RW	6	aev	
25	19	vsyncstartrow_f1_l	u	u	uuuuuuuu	RW	7	aev	
26	1A	vsyncstoprow_f1_h	2	02	xxx00010	RW	6	aev	
27	1B	vsyncstoprow_f1_l	u	u	uuuuuuuu	RW	7	aev	
28	1C	vsynccolumn_h	0	00	xxxx0000	RW	5	0	
29	1D	vsynccolumn_l	2	02	00000010	RW	5	0	
37	25	clkdiv	32	20	xx100000	RW	6	aev	Clock divider
41	29	pad_control3	0	00	00000000	RW	5	0	Pad control
42	2A	pad_control4	0	00	00000000	RW	5	0	Pad control
44	2C	pad_control6	0	00	00000000	RW	5	0	Pad control
48	30	strap_control	255	FF	11111111	RW	5	0	Strap control
79	4F	flicker_control1	u	u	uuuuuuuu	RW	5	0	Flicker control
89	59	fd_period_a_h	u	u	uuuuuuuu	RW	5	0	Flicker period for A state
90	5A	fd_period_a_m	u	u	uuuuuuuu	RW	5	0	
91	5B	fd_period_a_l	u	u	uuuuuuuu	RW	5	0	
92	5C	fd_period_b_h	1	01	00000001	RW	5	0	Flicker period for B state
93	5D	fd_period_b_m	u	u	uuuuuuuu	RW	5	0	
94	5E	fd_period_b_l	u	u	uuuuuuuu	RW	5	0	
104	68	iris_control	0	00	00000000	RW	5	0	Iris control
142	8E	led_control1	0	00	00000000	RW	5	0	Led control
143	8F	led_control2	1	01	00000001	RW	5	0	
144	90	led_lvth1	0	00	00000000	RW	5	0	Led control level th.1
145	91	led_lvth2	0	00	00000000	RW	5	0	Led control level th.2
146	92	led_frame	128	80	10000000	RW	5	0	Led frame control
147	93	mirs_pw	100	64	01100100	RW	5	0	Mirs pulse width
148	94	iris_pw	100	64	01100100	RW	5	0	Iris pulse width

(Group A)

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
256	00	DeviceID_H	48	30	00110000	RO	0	0	device ID
257	01	DeviceID_L	137	89	10001001	RO	0	0	
258	02	RevNumber	0	00	00000000	RO	0	0	revision number
259	03	bank	0	00	00000000	RO	5	0	Register group selector
277	15	bayer_control_01	5	05	00000101	RW	5	0	Bayer control
278	16	bayer_control_02	250	FA	11111010	RW	5	0	Bayer control
416	A0	front_black_ref0	0	00	00000000	RW	5	0	Front black control
417	A1	front_black_ref1	0	00	00000000	RW	5	0	
418	A2	front_black_ref2	0	00	00000000	RW	5	0	
419	A3	front_black_ref3	0	00	00000000	RW	5	0	
420	A4	front_black_ref4	0	00	00000000	RW	5	0	
421	A5	front_black_ref5	0	00	00000000	RW	5	0	
422	A6	front_black_min	255	FF	11111111	RW	5	0	
423	A7	front_black_max	127	7F	01111111	RW	5	0	
424	A8	front_black	0	00	00000000	RW	6	aev	
444	BC	inttime_h	1	01	00000001	RW	6	aev	Integration time (line)
445	BD	inttime_m	64	40	01000000	RW	6	aev	
446	BE	inttime_l	0	00	00000000	RW	6	aev	Integration time (column)
447	BF	globalgain	0	00	00000000	RW	6	aev	Analog gain
448	C0	digitalgain	64	40	01000000	RW	6	aev	Digital gain
471	D7	real_led_data	0	00	00000000	RO	0	0	Current CdS data

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▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
512	00	DeviceID_H	48	30	00110000	RO	0	0	device ID
513	01	DeviceID_L	137	89	10001001	RO	0	0	
514	02	RevNumber	0	00	00000000	RO	0	0	revision number
515	03	bank	0	00	00000000	RO	5	0	Register group selector
518	06	isp_func_2	0	00	00000000	RW	6	aev	Isp function control
520	08	isp_func_4	0	00	00000000	RW	6	aev	Isp function control
573	3D	ygm1_y0	0	00	00000000	RW	5	0	Y gamma1 coefficient
574	3E	ygm1_y1	12	0C	00001100	RW	5	0	
575	3F	ygm1_y2	32	20	00100000	RW	5	0	
576	40	ygm1_y3	47	2F	00101111	RW	5	0	
577	41	ygm1_y4	58	3A	00111010	RW	5	0	
578	42	ygm1_y5	75	4B	01001011	RW	5	0	
579	43	ygm1_y6	88	58	01011000	RW	5	0	
580	44	ygm1_y7	109	6D	01101101	RW	5	0	
581	45	ygm1_y8	127	7F	01111111	RW	5	0	
582	46	ygm1_y9	156	9C	10011100	RW	5	0	
583	47	ygm1_y10	180	B4	10110100	RW	5	0	
584	48	ygm1_y11	202	CA	11001010	RW	5	0	
585	49	ygm1_y12	221	DD	11011101	RW	5	0	
586	4A	ygm1_y13	239	EF	11101111	RW	5	0	
587	4B	ygm1_y14	255	FF	11111111	RW	5	0	
588	4C	ygm2_y0	0	00	00000000	RW	5	0	Y gamma2 coefficient
589	4D	ygm2_y1	17	11	00010001	RW	5	0	
590	4E	ygm2_y2	27	1B	00011011	RW	5	0	
591	4F	ygm2_y3	35	23	00100011	RW	5	0	
592	50	ygm2_y4	42	2A	00101010	RW	5	0	
593	51	ygm2_y5	55	37	00110111	RW	5	0	
594	52	ygm2_y6	66	42	01000010	RW	5	0	
595	53	ygm2_y7	86	56	01010110	RW	5	0	
596	54	ygm2_y8	104	68	01101000	RW	5	0	
597	55	ygm2_y9	135	87	10000111	RW	5	0	
598	56	ygm2_y10	163	A3	10100011	RW	5	0	
599	57	ygm2_y11	188	BC	10111100	RW	5	0	
600	58	ygm2_y12	212	D4	11010100	RW	5	0	
601	59	ygm2_y13	234	EA	11101010	RW	5	0	
602	5A	ygm2_y14	255	FF	11111111	RW	5	0	

(Group C – continued)

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▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
603	5B	cgm1_y0	0	00	00000000	RW	5	0	RGB gamma1 coefficient
604	5C	cgm1_y1	15	0F	00001111	RW	5	0	
605	5D	cgm1_y2	38	26	00100110	RW	5	0	
606	5E	cgm1_y3	55	37	00110111	RW	5	0	
607	5F	cgm1_y4	67	43	01000011	RW	5	0	
608	60	cgm1_y5	84	54	01010100	RW	5	0	
609	61	cgm1_y6	98	62	01100010	RW	5	0	
610	62	cgm1_y7	119	77	01110111	RW	5	0	
611	63	cgm1_y8	136	88	10001000	RW	5	0	
612	64	cgm1_y9	164	A4	10100100	RW	5	0	
613	65	cgm1_y10	187	BB	10111011	RW	5	0	
614	66	cgm1_y11	207	CF	11001111	RW	5	0	
615	67	cgm1_y12	224	E0	11100000	RW	5	0	
616	68	cgm1_y13	241	F1	11110001	RW	5	0	
617	69	cgm1_y14	255	FF	11111111	RW	5	0	
618	6A	cgm2_y0	0	00	00000000	RW	5	0	RGB gamma2 coefficient
619	6B	cgm2_y1	7	07	00000111	RW	5	0	
620	6C	cgm2_y2	13	0D	00001101	RW	5	0	
621	6D	cgm2_y3	19	13	00010011	RW	5	0	
622	6E	cgm2_y4	24	18	00011000	RW	5	0	
623	6F	cgm2_y5	34	22	00100010	RW	5	0	
624	70	cgm2_y6	44	2C	00101100	RW	5	0	
625	71	cgm2_y7	62	3E	00111110	RW	5	0	
626	72	cgm2_y8	79	4F	01001111	RW	5	0	
627	73	cgm2_y9	111	6F	01101111	RW	5	0	
628	74	cgm2_y10	142	8E	10001110	RW	5	0	
629	75	cgm2_y11	172	AC	10101100	RW	5	0	
630	76	cgm2_y12	200	C8	11001000	RW	5	0	
631	77	cgm2_y13	228	E4	11100100	RW	5	0	
632	78	cgm2_y14	255	FF	11111111	RW	5	0	
653	8D	y_weight	64	40	01000000	RW	6	aev	Y weight
657	91	ycontrast_ref0	64	40	01000000	RW	5	0	Dark Y contrast fitting control
658	92	ycontrast_ref1	64	40	01000000	RW	5	0	
659	93	ycontrast_ref2	64	40	01000000	RW	5	0	
660	94	ycontrast	64	40	01000000	RW	6	aev	
661	95	ybrightness_ref0	240	F0	11110000	RW	5	0	Dark Y brightness fitting control
662	96	ybrightness_ref1	0	00	00000000	RW	5	0	
663	97	ybrightness_ref2	0	00	00000000	RW	5	0	
664	98	ybrightness	0	00	00000000	RW	6	aev	

(Group C – continued)

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
672	A0	prvc_wx1_h	0	00	xxxxxx00	RW	5	0	Privacy window size control
673	A1	prvc_wx1_l	1	01	00000001	RW	5	0	
674	A2	prvc_wx2_h	2	02	xxxxxx10	RW	5	0	
675	A3	prvc_wx2_l	128	80	10000000	RW	5	0	
676	A4	prvc_wy1_h	0	00	xxxxxx00	RW	5	0	
677	A5	prvc_wy1_l	1	01	00000001	RW	5	0	
678	A6	prvc_wy2_h	0	00	xxxxxx00	RW	5	0	
679	A7	prvc_wy2_l	240	F0	11110000	RW	5	0	
680	A8	prvc_y	0	00	00000000	RW	5	0	YCbCr of privacy window
681	A9	prvc_cb	128	80	10000000	RW	5	0	
682	AA	prvc_cr	128	80	10000000	RW	5	0	
691	B3	ae_fwx1_h	0	00	xxxxxx00	RW	5	0	AE full window X start position
692	B4	ae_fwx1_l	1	01	00000001	RW	5	0	
693	B5	ae_fwx2_h	2	02	xxxxxx10	RW	5	0	AE full window X stop position
694	B6	ae_fwx2_l	208	D0	11010000	RW	5	0	
695	B7	ae_fwy1_h	0	00	xxxxxx00	RW	5	0	AE full window Y start position
696	B8	ae_fwy1_l	1	01	00000001	RW	5	0	
697	B9	ae_fwy2_h	1	01	xxxxxx01	RW	5	0	AE full window Y stop position
698	BA	ae_fwy2_l	224	E0	11100000	RW	5	0	
699	BB	ae_cwx1_h	0	00	xxxxxx00	RW	5	0	AE center window X start position
700	BC	ae_cwx1_l	241	F1	11110001	RW	5	0	
701	BD	ae_cwx2_h	1	01	xxxxxx01	RW	5	0	AE center window X stop position
702	BE	ae_cwx2_l	224	E0	11100000	RW	5	0	
703	BF	ae_cwy1_h	0	00	xxxxxx00	RW	5	0	AE center window Y start position
704	C0	ae_cwy1_l	161	A1	10100001	RW	5	0	
705	C1	ae_cwy2_h	1	01	xxxxxx01	RW	5	0	AE center window Y stop position
706	C2	ae_cwy2_l	64	40	01000000	RW	5	0	
707	C3	ae_xaxis_h	1	01	xxxxxx01	RW	5	0	AE window X axis
708	C4	ae_xaxis_l	105	69	01101001	RW	5	0	
709	C5	ae_yaxis_h	0	00	xxxxxx00	RW	5	0	AE window Y axis
710	C6	ae_yaxis_l	241	F1	11110001	RW	5	0	
711	C7	awb_wx1_h	0	00	xxxxxx00	RW	5	0	AWB window X start position
712	C8	awb_wx1_l	1	01	00000001	RW	5	0	
713	C9	awb_wx2_h	2	02	xxxxxx10	RW	5	0	AWB window X stop position
714	CA	awb_wx2_l	208	D0	11010000	RW	5	0	
715	CB	awb_wy1_h	0	00	xxxxxx00	RW	5	0	AWB window Y start position
716	CC	awb_wy1_l	1	01	00000001	RW	5	0	
717	CD	awb_wy2_h	1	01	xxxxxx01	RW	5	0	AWB window Y stop position
718	CE	awb_wy2_l	224	E0	11100000	RW	5	0	
728	D8	af_cwx1_h	0	00	xxxxxx00	RW	5	0	AF center window X start position
729	D9	af_cwx1_l	241	F1	11110001	RW	5	0	
730	DA	af_cwx2_h	1	01	xxxxxx01	RW	5	0	AF center window X stop position
731	DB	af_cwx2_l	224	E0	11100000	RW	5	0	
732	DC	af_cwy1_h	0	00	xxxxxx00	RW	5	0	AF center window Y start position
733	DD	af_cwy1_l	161	A1	10100001	RW	5	0	
734	DE	af_cwy2_h	1	01	xxxxxx01	RW	5	0	AF center window Y stop position
735	DF	af_cwy2_l	64	40	01000000	RW	5	0	
736	E0	af_cweight	8	08	xxx01000	RW	5	0	AF weight center
737	E1	af_edge_th	0	00	x0000000	RW	5	0	AF edge TH

(Group C – continued)

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
739	E3	md_yth1	64	40	01000000	RW	5	0	Y threshold1 for motion detection
740	E4	md_yth2	64	40	01000000	RW	5	0	Y threshold2 for motion detection
741	E5	md_yth3	64	40	01000000	RW	5	0	Y threshold3 for motion detection
742	E6	md_yth4	64	40	01000000	RW	5	0	Y threshold4 for motion detection
743	E7	md_diff1	64	40	01000000	RW	5	0	Difference1 for motion detection
744	E8	md_diff2	64	40	01000000	RW	5	0	Difference2 for motion detection
745	E9	md_diff3	64	40	01000000	RW	5	0	Difference3 for motion detection
746	EA	md_diff4	64	40	01000000	RW	5	0	Difference4 for motion detection
747	EB	md_interval	8	08	00001000	RW	5	0	Intervals of frames used for motion detection
748	EC	md_alarm_y	0	00	00000000	RW	5	0	YCbCr for Motion detection alarm
749	ED	md_alarm_cb	128	80	10000000	RW	5	0	
750	EE	md_alarm_cr	128	80	10000000	RW	5	0	
751	EF	md_alarmnumb	4	04	00000100	RW	5	0	Number of Motion detection alarm
752	F0	md_alarm_xlw	4	04	00000100	RW	5	0	X width of motion detection alarm
753	F1	md_alarm_ylw	4	04	00000100	RW	5	0	Y width of motion detection alarm
754	F2	md_alarmdur_h	0	00	00000000	RW	5	0	Period of motion detection alarm
755	F3	md_alarmdur_l	60	3C	00111100	RW	5	0	
756	F4	md_sleepdur_h	2	02	00000010	RW	5	0	Motion detection sleep
757	F5	md_sleepdur_l	58	3A	00111010	RW	5	0	
758	F6	md_section7	0	00	00000000	RW	5	0	Image section 7 for motion detection
759	F7	md_section6	0	00	00000000	RW	5	0	Image section 6 for motion detection
760	F8	md_section5	0	00	00000000	RW	5	0	Image section 5 for motion detection
761	F9	md_section4	0	00	00000000	RW	5	0	Image section 4 for motion detection
762	FA	md_section3	0	00	00000000	RW	5	0	Image section 3 for motion detection
763	FB	md_section2	0	00	00000000	RW	5	0	Image section 2 for motion detection
764	FC	md_section1	0	00	00000000	RW	5	0	Image section 1 for motion detection
765	FD	md_section0	0	00	00000000	RW	5	0	Image section 0 for motion detection

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▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
768	00	DeviceID_H	48	30	00110000	RO	0	0	device ID
769	01	DeviceID_L	137	89	10001001	RO	0	0	
770	02	RevNumber	0	00	00000000	RO	0	0	revision number
771	03	bank	0	00	00000000	RO	5	0	Register group selector
772	04	cs11_a	56	38	00111000	RW	5	0	Color saturation matrix fitting reference
773	05	cs12_a	28	1C	00011100	RW	5	0	
774	06	cs21_a	130	82	10000010	RW	5	0	
775	07	cs22_a	44	2C	00101100	RW	5	0	
776	08	cs11_b	35	23	00100011	RW	5	0	
777	09	cs12_b	0	00	00000000	RW	5	0	
778	0A	cs21_b	0	00	00000000	RW	5	0	
779	0B	cs22_b	39	27	00100111	RW	5	0	
780	0C	cs11_c	39	27	00100111	RW	5	0	
781	0D	cs12_c	130	82	10000010	RW	5	0	
782	0E	cs21_c	2	02	00000010	RW	5	0	
783	0F	cs22_c	36	24	00100100	RW	5	0	
784	10	lens_gainr_a	6	06	00000110	RW	5	0	Lens gain fitting reference
785	11	lens_gainb_a	0	00	00000000	RW	5	0	
786	12	lens_gainr_b	2	02	00000010	RW	5	0	
787	13	lens_gainb_b	0	00	00000000	RW	5	0	
788	14	lens_gainr_c	2	02	00000010	RW	5	0	
789	15	lens_gainb_c	0	00	00000000	RW	5	0	
790	16	axis_a	48	30	00110000	RW	5	0	CS matrix / lens gain fitting reference
791	17	axis_b	80	50	01010000	RW	5	0	
792	18	axis_c	94	5E	01011110	RW	5	0	
793	19	user_cs	56	38	00111000	RW	5	0	User CS gain
795	1B	wb_rgain_h	0	00	00000000	RW	6	aev	Normalized white balance gain
796	1C	wb_rgain_l	93	5D	01011101	RW	6	aev	
797	1D	wb_ggain_h	0	00	00000000	RW	6	aev	
798	1E	wb_ggain_l	64	40	01000000	RW	6	aev	
799	1F	wb_bgain_h	0	00	00000000	RW	6	aev	
800	20	wb_bgain_l	94	5E	01011110	RW	6	aev	
861	5D	periedge_gain	0	00	00000000	RW	5	0	Peripheral edge gain
869	65	dark_ec_pth0	4	04	00000100	RW	5	0	Dark edge clamp plus threshold filter control
870	66	dark_ec_pth1	4	04	00000100	RW	5	0	
871	67	dark_ec_pth2	4	04	00000100	RW	5	0	
872	68	dark_ec_pth	4	04	00000100	RW	6	aev	
873	69	dark_ec_mth0	4	04	00000100	RW	5	0	Dark edge clamp minus threshold filter control
874	6A	dark_ec_mth1	32	20	00100000	RW	5	0	
875	6B	dark_ec_mth2	48	30	00110000	RW	5	0	
876	6C	dark_ec_mth	4	04	00000100	RW	6	aev	
887	77	dark_dc0	0	00	00000000	RW	5	0	de-color dark filter
888	78	dark_dc1	8	08	00001000	RW	5	0	
889	79	dark_dc2	16	10	00010000	RW	5	0	
890	7A	dark_dc	0	00	00000000	RW	6	aev	

(Group D – continued)

▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
901	85	motion_monitor7	0	00	00000000	RO	0	0	Current motion detection indicator
902	86	motion_monitor6	0	00	00000000	RO	0	0	
903	87	motion_monitor5	0	00	00000000	RO	0	0	
904	88	motion_monitor4	0	00	00000000	RO	0	0	
905	89	motion_monitor3	0	00	00000000	RO	0	0	
906	8A	motion_monitor2	0	00	00000000	RO	0	0	
907	8B	motion_monitor1	0	00	00000000	RO	0	0	
908	8C	motion_monitor0	0	00	00000000	RO	0	0	
909	8D	af_edge_sum3	0	00	00000000	RO	0	0	Edge data for auto focus
910	8E	af_edge_sum2	0	00	00000000	RO	0	0	
911	8F	af_edge_sum1	0	00	00000000	RO	0	0	
912	90	af_edge_sum0	0	00	00000000	RO	0	0	
1009	F1	edge_gain_lf0	48	30	00110000	RW	5	0	edge gain lf dark filter fiting
1010	F2	edge_gain_lf1	48	30	00110000	RW	5	0	
1011	F3	edge_gain_lf2	48	30	00110000	RW	5	0	
1012	F4	edge_gain_lf	48	30	00110000	RW	6	aev	

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▶ Register Tables – Group E

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1024	00	DeviceID_H	48	30	00110000	RO	0	0	device ID
1025	01	DeviceID_L	137	89	10001001	RO	0	0	
1026	02	RevNumber	0	00	00000000	RO	0	0	revision number
1027	03	bank	0	00	00000000	RO	5	0	Register group selector
1028	04	auto_control_1	152	98	10011000	RW	6	autov	Auto control
1042	12	expfrmh_h	2	02	00000010	RW	5	0	AE reference
1043	13	expfrmh_l	u	u	uuuuuuuu	RW	5	0	
1044	14	midfrmheight_h	2	02	00000010	RW	5	0	
1045	15	midfrmheight_l	u	u	uuuuuuuu	RW	5	0	
1046	16	maxfrmheight_h	2	02	00000010	RW	5	0	
1047	17	maxfrmheight_l	u	u	uuuuuuuu	RW	5	0	
1048	18	minexp_h	0	00	00000000	RW	5	0	
1049	19	minexp_m	0	00	00000000	RW	5	0	
1050	1A	minexp_l	40	28	00101000	RW	5	0	
1051	1B	midexp_t	2	02	00000010	RW	5	0	
1052	1C	midexp_h	71	47	01000111	RW	5	0	
1053	1D	midexp_m	224	E0	11100000	RW	5	0	
1054	1E	maxexp_t	4	04	00000100	RW	5	0	
1055	1F	maxexp_h	143	8F	10001111	RW	5	0	
1056	20	maxexp_m	192	C0	11000000	RW	5	0	
1058	22	ext_inttime_h	0	00	00000000	RW	6	autov	Manual integration time @ external AE mode
1059	23	ext_inttime_m	128	80	10000000	RW	6	autov	
1060	24	ext_inttime_l	0	00	00000000	RW	6	autov	
1061	25	ext_glbg_h	1	01	00000001	RW	6	autov	Manual analog gain @ external AE mode
1062	26	ext_glbg_l	0	00	00000000	RW	6	autov	
1063	27	exposure_t	0	00	00000000	RW	6	autov	Exposure
1064	28	exposure_h	1	01	00000001	RW	6	autov	
1065	29	exposure_m	64	40	01000000	RW	6	autov	
1066	2A	exposure_l	0	00	00000000	RW	6	autov	
1072	30	ae_weight1	8	08	xx001000	RW	5	0	AE weight peripheral
1073	31	ae_weight2	8	08	xx001000	RW	5	0	
1074	32	ae_weight3	8	08	xx001000	RW	5	0	
1075	33	ae_weight4	8	08	xx001000	RW	5	0	
1076	34	ae_weightc	8	08	xx001000	RW	5	0	AE weight center
1081	39	ymean_h	0	00	00000000	RW	5	0	Y mean
1082	3A	ymean_l	128	80	10000000	RW	5	0	
1083	3B	max_yt1	152	98	10011000	RW	6	autov	Min / max ytarget control reference
1084	3C	max_yt2	80	50	01010000	RW	6	autov	
1085	3D	min_yt1	152	98	10011000	RW	6	autov	
1086	3E	min_yt2	80	50	01010000	RW	6	autov	
1095	47	user_wyt	128	80	10000000	RW	6	autov	User weight Y target
1096	48	ae_up_speed	4	04	00000100	RW	6	autov	AE upside speed
1097	49	ae_down_speed	4	04	00000100	RW	6	autov	AE downside speed
1098	4A	ae_lock	5	05	00000101	RW	6	autov	AE lock range

(Group E – continued)

▶ Register Tables – Group E

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1128	68	rg_ratio_a	128	80	10000000	RW	5	0	Target awb ratio fitting reference
1129	69	bg_ratio_a	128	80	10000000	RW	5	0	
1130	6A	rg_ratio_b	128	80	10000000	RW	5	0	
1131	6B	bg_ratio_b	128	80	10000000	RW	5	0	
1132	6C	rg_ratio_c	128	80	10000000	RW	5	0	
1133	6D	bg_ratio_c	128	80	10000000	RW	5	0	
1134	6E	ratio_axis_a	48	30	00110000	RW	5	0	
1135	6F	ratio_axis_b	80	50	01010000	RW	5	0	
1136	70	ratio_axis_c	94	5E	01011110	RW	5	0	
1137	71	awb_rgratio	128	80	10000000	RW	5	0	AWB RG ratio control
1138	72	awb_bgratio	128	80	10000000	RW	5	0	AWB BG ratio control
1139	73	awb_lock	6	06	00000110	RW	5	0	AWB lock range
1140	74	awb_speed	4	04	00000100	RW	5	0	AWB speed
1141	75	awb_rgain_min1	0	00	00000000	RW	5	0	AWB gain clamping fitting control
1142	76	awb_rgain_min2	0	00	00000000	RW	5	0	
1143	77	awb_rgain_max1	255	FF	11111111	RW	5	0	
1144	78	awb_rgain_max2	255	FF	11111111	RW	5	0	
1145	79	awb_bgain_min1	0	00	00000000	RW	5	0	
1146	7A	awb_bgain_min2	0	00	00000000	RW	5	0	
1147	7B	awb_bgain_max1	255	FF	11111111	RW	5	0	
1148	7C	awb_bgain_max2	255	FF	11111111	RW	5	0	
1149	7D	awb_cmp_th1_h	0	00	00000000	RW	5	0	
1150	7E	awb_cmp_th1_m	128	80	10000000	RW	5	0	
1151	7F	awb_cmp_th2_h	1	01	00000001	RW	5	0	
1152	80	awb_cmp_th2_m	0	00	00000000	RW	5	0	
1154	82	filter_ctrl_1	240	F0	11110000	RW	6	autov	filter control
1165	8D	dark_xref1_g0_h	0	00	00000000	RW	5	0	Dark filter x-axis reference
1166	8E	dark_xref1_g0_l	6	06	00000110	RW	5	0	
1167	8F	dark_xref2_g0_h	0	00	00000000	RW	5	0	
1168	90	dark_xref2_g0_l	16	10	00010000	RW	5	0	
1169	91	dark_xref3_g0_h	0	00	00000000	RW	5	0	
1170	92	dark_xref3_g0_l	32	20	00100000	RW	5	0	
1179	9B	totalgain_h	0	00	00000000	RW	6	autov	Total gain
1180	9C	totalgain_l	1	01	00000001	RW	6	autov	

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▶ Register Tables – Group F

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1280	00	DeviceID_H	48	30	00110000	RO	0	0	device ID
1281	01	DeviceID_L	137	89	10001001	RO	0	0	
1282	02	RevNumber	0	00	00000000	RO	0	0	revision number
1283	03	bank	0	00	00000000	RO	5	0	Register group selector
1284	04	pg_control0	9	09	00001001	RW	6	aev	Embedded parking guide line control
1285	05	pg_control1	0	00	00000000	RW	6	aev	Embedded parking guide line control
1286	06	pg_control2	0	00	00000000	RW	6	aev	Embedded parking guide line control
1288	08	pg_yt	127	7F	01111111	RW	6	aev	Embedded parking guide line control
1289	09	pg_y1	115	73	01110011	RW	6	aev	
1290	0A	pg_y2	2	02	00000010	RW	6	aev	
1291	0B	pg_y3	8	08	00001000	RW	6	aev	
1292	0C	pg_y4	15	0F	00001111	RW	6	aev	
1293	0D	pg_y5	25	19	00011001	RW	6	aev	
1294	0E	pg_y6	37	25	00100101	RW	6	aev	
1295	0F	pg_y7	40	28	00101000	RW	6	aev	
1296	10	pg_y8	56	38	00111000	RW	6	aev	
1297	11	pg_y9	78	4E	01001110	RW	6	aev	
1298	12	pg_y10	82	52	01010010	RW	6	aev	
1299	13	pg_a	143	8F	10001111	RW	6	aev	
1300	14	pg_b	100	64	01100100	RW	6	aev	
1301	15	pg_c	191	BF	10111111	RW	6	aev	
1302	16	pg_d	7	07	00000111	RW	6	aev	
1303	17	pg_e	12	0C	00001100	RW	6	aev	
1304	18	pg_f	21	15	00010101	RW	6	aev	
1305	19	pg_line1	33	21	00100001	RW	6	aev	
1306	1A	pg_line2	35	23	00100011	RW	6	aev	
1307	1B	pg_line3	36	24	00100100	RW	6	aev	
1308	1C	pg_line4	70	46	01000110	RW	6	aev	
1309	1D	pg_line5	72	48	01001000	RW	6	aev	
1310	1E	pg_line6	66	42	01000010	RW	6	aev	
1311	1F	pg_line7	75	4B	01001011	RW	6	aev	
1312	20	pg_line8	113	71	01110001	RW	6	aev	
1313	21	pg_line9	99	63	01100011	RW	6	aev	
1314	22	pg_line10	116	74	01110100	RW	6	aev	
1315	23	pg_center_h	1	01	xxxxxx01	RW	6	aev	
1316	24	pg_center_l	104	68	01101000	RW	6	aev	
1317	25	pg_l_type_h	1	01	xxxxxx01	RW	6	aev	
1318	26	pg_l_type_l	33	21	00100001	RW	6	aev	
1319	27	pg_hl_en_h	0	00	xxxxxx00	RW	6	aev	
1320	28	pg_hl_en_l	0	00	00000000	RW	6	aev	
1321	29	pg_cl_x_h	0	00	xxxxxx00	RW	5	0	Embedded parking guide line control
1322	2A	pg_cl_x_l	0	00	00000000	RW	5	0	
1323	2B	pg_cl_y	0	00	00000000	RW	5	0	
1324	2C	pg_cl_h_stop_h	0	00	xxxxxxx0	RW	5	0	
1325	2D	pg_cl_h_stop_l	0	00	00000000	RW	5	0	
1326	2E	pg_cl_w	0	00	00000000	RW	5	0	
1327	2F	pg_cl_hght	0	00	00000000	RW	5	0	
1328	30	pg_cbl_hght	0	00	00000000	RW	5	0	

(Group F – continued)

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▶ Register Tables – Group F

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1329	31	pg_cl_wweight	0	00	00000000	RW	5	0	Embedded parking guide line control
1330	32	pg_cl_hweight	0	00	00000000	RW	5	0	
1332	34	pg_string0_x_h	1	01	xxxxxxx1	RW	5	0	Embedded PG string position
1333	35	pg_string0_x_l	255	FF	11111111	RW	5	0	
1334	36	pg_string1_x_h	1	01	xxxxxxx1	RW	5	0	
1335	37	pg_string1_x_l	255	FF	11111111	RW	5	0	
1336	38	pg_string2_x_h	1	01	xxxxxxx1	RW	5	0	
1337	39	pg_string2_x_l	255	FF	11111111	RW	5	0	
1338	3A	pg_string3_x_h	1	01	xxxxxxx1	RW	5	0	
1339	3B	pg_string3_x_l	255	FF	11111111	RW	5	0	
1340	3C	pg_string4_x_h	1	01	xxxxxxx1	RW	5	0	
1341	3D	pg_string4_x_l	255	FF	11111111	RW	5	0	
1342	3E	pg_string5_x_h	1	01	xxxxxxx1	RW	5	0	
1343	3F	pg_string5_x_l	255	FF	11111111	RW	5	0	
1344	40	pg_string6_x_h	1	01	xxxxxxx1	RW	5	0	
1345	41	pg_string6_x_l	255	FF	11111111	RW	5	0	
1346	42	pg_string7_x_h	1	01	xxxxxxx1	RW	5	0	
1347	43	pg_string7_x_l	255	FF	11111111	RW	5	0	
1348	44	pg_string0_y_h	1	01	xxxxxxx1	RW	5	0	
1349	45	pg_string0_y_l	255	FF	11111111	RW	5	0	
1350	46	pg_string1_y_h	1	01	xxxxxxx1	RW	5	0	
1351	47	pg_string1_y_l	255	FF	11111111	RW	5	0	
1352	48	pg_string2_y_h	1	01	xxxxxxx1	RW	5	0	
1353	49	pg_string2_y_l	255	FF	11111111	RW	5	0	
1354	4A	pg_string3_y_h	1	01	xxxxxxx1	RW	5	0	
1355	4B	pg_string3_y_l	255	FF	11111111	RW	5	0	
1356	4C	pg_string4_y_h	1	01	xxxxxxx1	RW	5	0	
1357	4D	pg_string4_y_l	255	FF	11111111	RW	5	0	
1358	4E	pg_string5_y_h	1	01	xxxxxxx1	RW	5	0	
1359	4F	pg_string5_y_l	255	FF	11111111	RW	5	0	
1360	50	pg_string6_y_h	1	01	xxxxxxx1	RW	5	0	
1361	51	pg_string6_y_l	255	FF	11111111	RW	5	0	
1362	52	pg_string7_y_h	1	01	xxxxxxx1	RW	5	0	
1363	53	pg_string7_y_l	255	FF	11111111	RW	5	0	
1364	54	pg_string0_ch0	0	00	xxxx0000	RW	5	0	Embedded PG character selection in strings
1365	55	pg_string0_ch2	0	00	xxxx0000	RW	5	0	
1366	56	pg_string1_ch0	0	00	xxxx0000	RW	5	0	
1367	57	pg_string1_ch2	0	00	xxxx0000	RW	5	0	
1368	58	pg_string2_ch0	0	00	xxxx0000	RW	5	0	
1369	59	pg_string2_ch2	0	00	xxxx0000	RW	5	0	
1370	5A	pg_string3_ch0	0	00	xxxx0000	RW	5	0	
1371	5B	pg_string3_ch2	0	00	xxxx0000	RW	5	0	
1372	5C	pg_string4_ch0	0	00	xxxx0000	RW	5	0	
1373	5D	pg_string4_ch2	0	00	xxxx0000	RW	5	0	
1374	5E	pg_string5_ch0	0	00	xxxx0000	RW	5	0	
1375	5F	pg_string5_ch2	0	00	xxxx0000	RW	5	0	
1376	60	pg_string6_ch0	0	00	xxxx0000	RW	5	0	
1377	61	pg_string6_ch2	0	00	xxxx0000	RW	5	0	
1378	62	pg_string7_ch0	0	00	xxxx0000	RW	5	0	
1379	63	pg_string7_ch2	0	00	xxxx0000	RW	5	0	

(Group F – continued)

▶ Register Tables – Group F

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1435	9B	blink_frame	0	00	00000000	RW	5	0	OSD blink control
1436	9C	blink_control	0	00	xxxx0000	RW	5	0	
1437	9D	spi_osd_bndry	0	00	00000000	RW	5	0	OSD boundary
1474	C2	sw_comp1_h	0	00	00000000	RW	5	0	Switch comparing for Embedded OSD control
1475	C3	sw_comp1_l	31	1F	00011111	RW	5	0	
1476	C4	sw_comp2_h	0	00	00000000	RW	5	0	
1477	C5	sw_comp2_l	30	1E	00011110	RW	5	0	
1478	C6	sw_comp3_h	0	00	00000000	RW	5	0	
1479	C7	sw_comp3_l	28	1C	00011100	RW	5	0	
1480	C8	sw_comp4_h	0	00	00000000	RW	5	0	
1481	C9	sw_comp4_l	24	18	00011000	RW	5	0	
1482	CA	sw_comp5_h	0	00	00000000	RW	5	0	
1483	CB	sw_comp5_l	16	10	00010000	RW	5	0	
1516	EC	sif_state	0	00	00000000	RO	0	0	SIF state
1517	ED	monitor_switch	0	00	00000000	RO	0	0	Monitoring sampled switch level for embedded OSD control

▶ Register Tables – Group H

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1792	00	DeviceID_H	48	30	00110000	RO	0	0	device ID
1793	01	DeviceID_L	137	89	10001001	RO	0	0	
1794	02	RevNumber	0	00	00000000	RO	0	0	revision number
1795	03	bank	0	00	00000000	RO	5	0	Register group selector
1796	04	sync_blankEAV_f0	182	B6	10110110	RW	5	0	Blank EAV for field0 of CCIR656 data or blank EAV for frame data
1797	05	sync_blankSAV_f0	171	AB	10101011	RW	5	0	Blank EAV for field1 of CCIR656 data or blank EAV for frame data
1798	06	sync_activeEAV_f0	157	9D	10011101	RW	5	0	Active EAV for field0 of CCIR656 data or active EAV for frame data
1799	07	sync_activeSAV_f0	128	80	10000000	RW	5	0	Active EAV for field1 of CCIR656 data or active EAV for frame data
1800	08	sync_blankEAV_f1	241	F1	11110001	RW	5	0	blank EAV for field1 of CCIR656 data
1801	09	sync_blankSAV_f1	236	EC	11101100	RW	5	0	blank SAV for field1 of CCIR656 data
1802	0A	sync_activeEAV_f1	218	DA	11011010	RW	5	0	Active EAV for field1 of CCIR656 data
1803	0B	sync_activeSAV_f1	199	C7	11000111	RW	5	0	Active SAV for field1 of CCIR656 data
1804	0C	sync_CCIR_FF	255	FF	11111111	RW	5	0	CCIR data format
1805	0D	sync_CCIR_00	0	00	00000000	RW	5	0	
1806	0E	sync_CCIR_80	128	80	10000000	RW	5	0	
1807	0F	sync_CCIR_10	16	10	00010000	RW	5	0	
1813	15	osd_opac0	16	10	xxx10000	RW	5	0	OSD layer0 transparency
1814	16	osd_opac1	16	10	xxx10000	RW	5	0	OSD layer1 transparency
1815	17	osd_opac2	16	10	xxx10000	RW	5	0	OSD layer2 transparency
1816	18	osd_opac3	16	10	xxx10000	RW	5	0	OSD layer3 transparency
1817	19	hlight_opac	16	10	xxx10000	RW	5	0	Highlight zone transparency
1949	9D	enc_control1	0	00	00000000	RW	5	0	Encoder mode
1953	A1	osd_init_s	18	12	00010010	RW	5	0	UTC data sampling control
1954	A2	pelco_sync_s	24	18	00011000	RW	5	0	
1955	A3	osd_init_w	4	04	xxx00100	RW	5	0	
1956	A4	pelco_efline_h	0	00	xxxxxx00	RW	5	0	
1957	A5	pelco_efline_l	19	13	00010011	RW	5	0	
1958	A6	pelco_ofline_h	0	00	xxxxxx00	RW	5	0	
1959	A7	pelco_ofline_l	19	13	00010011	RW	5	0	
1961	A9	setup_w	7	07	xxx00111	RW	5	0	Setup time width
1962	AA	hsync_p_toffset	0	00	xxx00000	RW	5	0	Stop point of hsync
1963	AB	burst_duration	0	00	00000000	RW	5	0	Burst duration
1964	AC	burst_slope_step	56	38	00111000	RW	5	0	

(Group H – continued)

1/3 inch NTSC/PAL CMOS Image Sensor with 720 X 480 Pixel Array

▶ Register Tables – Group H

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1965	AD	l_blank_start	0	00	00000000	RW	5	0	Line blanking interval
1966	AE	l_blank_stop	0	00	00000000	RW	5	0	
1967	AF	sync_rising	1	01	xxxx0001	RW	5	0	horizontal rising time control of composite signal
1975	B7	enc_mode	u	u	uuuuuuuu	RW	5	0	Encoder mode
1976	B8	enc_sync	16	10	00010000	RW	5	0	Encoder sync level
1977	B9	enc_blankH	0	00	00000000	RW	5	0	Encoder blank level
1978	BA	enc_blankL	u	u	uuuuuuuu	RW	5	0	
1979	BB	enc_pedestal	u	u	uuuuuuuu	RW	5	0	Encoder pedestal
1980	BC	enc_burst	u	u	uuuuuuuu	RW	5	0	Burst amplitude
1981	BD	enc_Ygain	u	u	uuuuuuuu	RW	5	0	Y convergence gain from YCbCr to YUV
1982	BE	enc_Ugain	u	u	uuuuuuuu	RW	5	0	U convergence gain from YCbCr to YUV
1983	BF	enc_Vgain	u	u	uuuuuuuu	RW	5	0	V convergence gain from YCbCr to YUV
1984	C0	enc_Yrange_H	3	03	xxxxx011	RW	5	0	Max. luminance
1985	C1	enc_Yrange_L	32	20	00100000	RW	5	0	
1986	C2	enc_Crange_H	1	01	xxxxx001	RW	5	0	Max. amplitudes of chrominance
1987	C3	enc_Crange_L	u	u	uuuuuuuu	RW	5	0	
1988	C4	enc_chroma_max_H	3	03	xxxxx011	RW	5	0	Maximum chrominance of composite output
1989	C5	enc_chroma_max_L	u	u	uuuuuuuu	RW	5	0	
1990	C6	enc_chroma_min_H	0	00	xxxxx000	RW	5	0	Minimum chrominance of composite output
1991	C7	enc_chroma_min_L	u	u	uuuuuuuu	RW	5	0	
2022	E6	burst_toffset	0	00	00000000	RW	5	0	Burst time +/- offset
2023	E7	dac_clk_control	0	00	00000000	RW	5	0	DAC clock control
2024	E8	resol_th	0	00	00000000	RW	5	0	Resolution enhance threshold
2025	E9	enc_stdby_fcnt	1	01	00000001	RW	5	0	data kill delay at standby mode
2026	EA	enc_initset_fcnt	1	01	00000001	RW	5	0	data kill delay after initialization
2027	EB	encdat_rising	1	01	xxxx0001	RW	5	0	edge of the line blanking pulse rising time control
2028	EC	enc_scfreq	u	u	uuuuuuuu	RW	5	0	Subcarrier frequency selection for which TV mode

< Group A >

▶ Register Tables (Detailed) : Group A

Register names are written in *slanted* characters. To differentiate between decimal, binary, and hexa numbers, (d, b, and h) are appended. The sensor should be reset by RSTB pin set low, after power is up, for at least 16 master clock periods. This will initialize all of the registers to their default values. Default values of 'U' are wire-strapping registers.

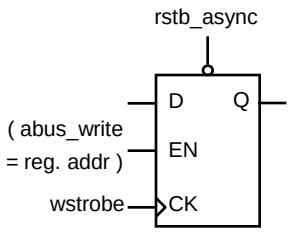
There are two register type.

1. Available Read Only (indicator is RO).
2. Available Read and Write (indicator is RW).

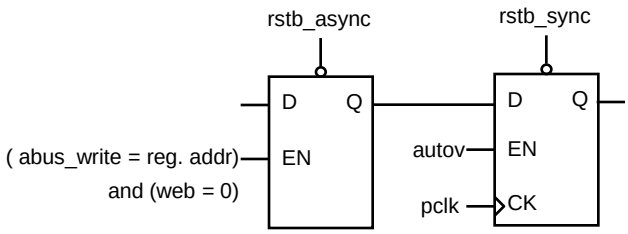
In addition, RW type register can be grouped by stage. There are 3 register stage.

1. 1 stage register (indicator is [5, 0]).
2. 2 stage register which is updated at auto vsync falling edge (indicator is [6, autov]).
3. 2 stage register which is updated at ae vsync falling edge (indicator is [6, aev]).
4. 2 stage register which is updated at ae vsync falling edge (indicator is [7, aev]) → this is 2 flip-flop structure.

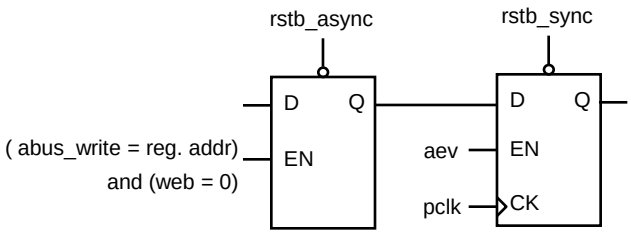
Below figure shows block diagram by register stage.



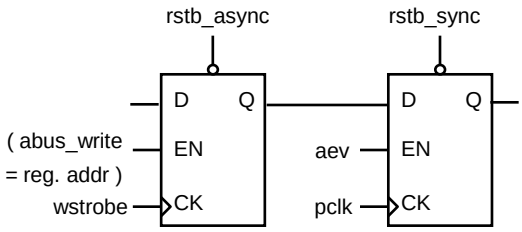
1. [1 stage register]



2. [2 stage register @ autov]



3. [2 stage register @ aev]



4. [2 stage register @ aev]

Where, abus_write means user input address by 2-wire serial interface. wstrobe and web is generated by SSCL pin. pclk means pixel clock for core. aev means ae vsync falling edge. autov means auto vsync falling edge. For more information of ae vsync and auto vsync, please refer to Reg. C-ACh~B1h.

< Group A >

< Group A >

(0~3) DeviceID, RevNumber, Register Selector

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
0	00	DeviceID_H	48	30	00110000	RO	0	0	device ID
1	01	DeviceID_L	137	89	10001001	RO	0	0	
2	02	RevNumber	0	00	00000000	RO	0	0	revision number
3	03	bank	0	00	xxxx0000	RW	5	0	Register group selector

▷ DeviceID, RevNumber, Register Selector

PC3089N device ID, reversion number, Register Selector.

Register Group A(00h) / B(01h) / C(02h) / D(03h) / E(04h) / F(05h) / G(06h) / H(07h)

(4) Chip mode

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
4	04	chip_mode	u	u	uuuuuuuu	RW	7	aev	chip mode selection(NTSC, PAL, VGA)

register name : chip_mdoe								
register #	bit#	name	default	**U**	default(h)	**UU**	default(b)	**xxxxxxuu**
04d (04h)	7	x	0	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2	x	0	Reserved				
	1	chip_mode	U	Chip mode selection 00b - NTSC, (M)PAL 01b - PAL else – 960h				
	0		U					

▷ chip_mode

default value : U ➔ wire-strapping register

Chip mode selection

The default value of this register is changed by wire-strapping.

After initialize of wire-strapping, the register can be set with other values through I2C communication.

< Group A >

(5) Mirror

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
5	05	mirror	u	u	uuuuuuuu	RW	7	aev	Mirror

register name : mirror								
register #	bit#	name	default	**U**	default(h)	**UU**	default(b)	**xxxxxxuu**
05d (05h)	7	x	0	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2	x	0	Reserved				
	1	vm	U	Vertical mirror ON/OFF				
	0	hm	U	Horizontal mirror ON/OFF				

▷ vm/hm

default value : U ➔ wire-strapping register

The default value of this register is changed by wire-strapping.

After initialize of wire-strapping, the register can be set with other values through I2C communication.

< Group A >

(6~11) FrameWidth, FrameHeight

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
6	06	framewidth_h	u	u	uuuuuuuu	RW	7	aev	Framewidth
7	07	framewidth_l	u	u	uuuuuuuu	RW	7	aev	
8	08	fd_fheight_a_h	2	02	xxx00010	RW	6	aev	Frameheight
9	09	fd_fheight_a_l	u	u	uuuuuuuu	RW	7	aev	
10	0A	fd_fheight_b_h	2	02	xxx00010	RW	6	aev	
11	0B	fd_fheight_b_l	u	u	uuuuuuuu	RW	7	aev	

▷ FrameWidth, FrameHeight

default value : U ➔ wire-strapping register

FrameWidth is the number of columns to be counted during one line time. FrameHeight is the number of rows. Column(Row) counter value is incremented 1 by 1 until it reaches FrameWidth(FrameHeight), then it is reset to 0. FrameHeight and FrameWidth determines the frame rate. Frame rate is given as follows.

Frame Rate = freq (pclk) / ((FrameHeight +1) X (FrameWidth+1))

For example, If Pixel clock (pclk) = 13.5MHz, FrameHeight = 857d and FrameWidth = 524d. then, the frame rate is 30 fps for 720x480 Mode. If you double the Frame Height , you cut the frame rate by half.

▶ fd_fheight_a : flicker A state frameheight
▶ fd_fheight_b : flicker B state frameheight

< Group A >

(12~19) Window

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
12	0C	windowx1_h	0	00	xxxxxx00	RW	6	aev	Window
13	0D	windowx1_l	1	01	00000001	RW	6	aev	
14	0E	windowy1_h	0	00	xxxxxx00	RW	6	aev	
15	0F	windowy1_l	1	01	00000001	RW	6	aev	
16	10	windowx2_h	2	02	xxxxxx10	RW	6	aev	
17	11	windowx2_l	208	D0	11010000	RW	6	aev	
18	12	windowy2_h	1	01	xxxxxx01	RW	6	aev	
19	13	windowy2_l	224	E0	11100000	RW	6	aev	

▷ Window

Window can be defined by 4 parameters : WindowX1, WindowY1, WindowX2, and WindowY2. Serial image data stream out pixel by pixel. Window specifies the area of pixels that we are interested in. Hsync signal indicates if the image data output is from a pixel that lies within the window area or not. Output data stream does not stop for pixels lying outside the window : just the Hsync signal is de-asserted.

The actual window position in the frame is given as

upper right corner = (Window X1 + 1, Window Y1)
lower left corner = (Window X2, Window Y2 - 1)

< Group A >

< Group A >

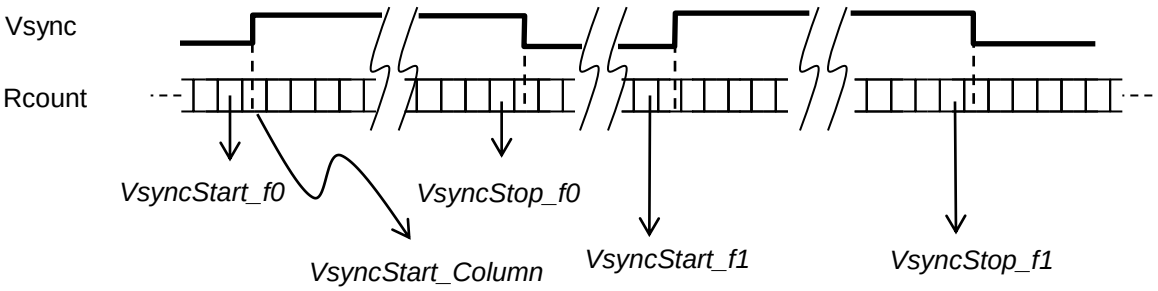
(20~29) Vsync Row Start/Stop, Vsync Column Start

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
20	14	vsyncstartrow_f0_h	0	00	xxx00000	RW	6	aev	Vsync generation
21	15	vsyncstartrow_f0_l	23	17	00010111	RW	6	aev	
22	16	vsyncstoprow_f0_h	1	01	xxx00001	RW	6	aev	
23	17	vsyncstoprow_f0_l	u	u	uuuuuuuu	RW	7	aev	
24	18	vsyncstartrow_f1_h	1	01	xxx00001	RW	6	aev	
25	19	vsyncstartrow_f1_l	u	u	uuuuuuuu	RW	7	aev	
26	1A	vsyncstoprow_f1_h	2	02	xxx00010	RW	6	aev	
27	1B	vsyncstoprow_f1_l	u	u	uuuuuuuu	RW	7	aev	
28	1C	vsynccolumn_h	0	00	xxxx0000	RW	5	0	
29	1D	vsynccolumn_l	2	02	00000010	RW	5	0	

▷ Output Vsync Generation

default value : U ➔ wire-strapping register

Output Vsync Row Start/Stop points and Column Start point



< Group A >

(37) Clock divider

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
37	25	clkdiv	32	20	xx100000	RW	6	aev	Clock divider

▷ **Clock divider**

clkdiv[2:0]	ppclk
000b	mclk
001b	mclk * 2/3
010b	mclk * 1/2
011b	mclk * 1/3
100b	mclk * 1/4
101b	mclk * 1/8
else	mclk

clkdiv[4:3]	mclk
00b	vco
01b	vco * 1/2
10b	vco * 1/3
11b	vco * 1/4

clkdiv[5]	pclk
0b	ppclk/2
1b	ppclk

◆ explain clocks.
→ pclk : The counter values increase at the pace of pclk.
ppclk: essential clock for internal operation.
mclk: main clock.

< Group A >

(41) Pad_control3

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
41	29	pad_control3	0	00	00000000	RW	5	0	Pad control

register name : pad_control3								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
41d (29h)	7	vsync_pad_en	0	Vsync pad 0b : disable ,1b : enable				
	6	hsync_drv	0	Hsync drivability control				
	5		0					
	4	hsync_pad_en	0	Hsync pad 0b : disable ,1b : enable				
	3	d1_pad_en	0	Data1 pad 0b : disable ,1b : enable				
	2	d0_pad_en	0	Data0 pad 0b : disable, 1b : enable				
	1	d0_pad_selection	0	Data0 pad selection bit 0b : DO0, 1b : motion detection				
	0	d_pad_selection	0	Data pad selection bit 0b : ISP data, 1b : manual(pad_control9)				

(42) Pad_control4

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
42	2A	pad_control4	0	00	00000000	RW	5	0	Pad control

register name : pad_control4								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
42d (2Ah)	7	ledctrl_en	0	LED pad 0b : disable ,1b : enable				
	6	ledctrl_pad_drv	0	LED pad drivability control				
	5		0					
	4	x	0	Reserved				
	3	x	0	Reserved				
	2		0					
	1		0					
	0		0					

(44) Pad_control6

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
44	2C	pad_control6	0	00	00000000	RW	5	0	Pad control

register name : pad_control6								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
44d (2Ch)	7	mirsctrl_en	0	MIRS output pad				
	6	mirsctrl_pad_drv	0	MIRS output pad drivability control				
	5		0					
	4	irisctrl_en	0	Iris output pad				
	3	irisctrl_pad_drv	0	Iris output pad drivability control				
	2		0					
	1	x	0	Reserved				
	0	x	0	Reserved				

(48) Strap_control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
48	30	strap_control	255	FF	11111111	RW	5	0	Strap control

register name : strap_control								
register #	bit#	name	default	**255**	default(h)	**FF**	default(b)	**11111111**
48d (30h)	7	Strap master	1	I2C master strap control mode 1b : control when reset='0' ,0b : control in real-time				
	6	Strap General	1	General strap control mode 1b : control when reset='0' ,0b : control in real-time				
	5	OSD	1	OSD strap control mode 1b : control when reset='0' ,0b : control in real-time				
	4	Indoor / Outdoor	1	Indoor/Outdoor strap control mode 1b : control when reset='0' ,0b : control in real-time				
	3	BLC	1	BLC strap control mode 1b : control when reset='0' ,0b : control in real-time				
	2	Strap flicker	1	Flicker cancellation strap control mode 1b : control when reset='0' ,0b : control in real-time				
	1	Strap TV mode	1	TV mode strap control mode 1b : control when reset='0' ,0b : control in real-time				
	0	Strap Mirror	1	Horizontal & Vertical Mirror strap control mode 1b : control when reset='0' ,0b : control in real-time				

▷ **Strap control**

Strap_control= "FF"(default): It will be applies only to strap values before reset.

Strap_control= "00h": It can be real time control of strap.

< Group A >

(79) Flicker control 1

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
79	4F	flicker_control1	u	u	uuuuuuuu	RW	5	0	Flicker control

register name : flicker_control1								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
79d (4Fh)	7	x	1	reserved				
	6	x	0	reserved				
	5	x	0	reserved				
	4	x	0	reserved				
	3	manual_A	0	manual_A				
	2	manual_B	0	manual_B				
	1	x	0	reserved				
	0		0					

▷ **manual_A**

For 60hz light source

▷ **manual_B**

For 50hz light source

.

< Group A >

< Group A >

(80~96) Flicker control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
89	59	fd_period_a_h	u	u	uuuuuuuu	RW	5	0	Flicker period for A state
90	5A	fd_period_a_m	u	u	uuuuuuuu	RW	5	0	
91	5B	fd_period_a_l	u	u	uuuuuuuu	RW	5	0	
92	5C	fd_period_b_h	1	01	00000001	RW	5	0	Flicker period for B state
93	5D	fd_period_b_m	u	u	uuuuuuuu	RW	5	0	
94	5E	fd_period_b_l	u	u	uuuuuuuu	RW	5	0	

▷ Flicker period A & B

default value : U ➔ wire-strapping register

fd_period_A can be programmed by flicker period for 1/120 sec.

fd_period_B can be programmed by flicker period for 1/100 sec.

Flicker period for 1/120 sec and 1/100 sec are calculated by as below.

$$fd\_period\_a = \frac{256\text{d}^* \text{ pclk FREQ.}}{120\text{d} * framewidth}$$

$$fd\_period\_b = \frac{256\text{d}^* \text{ pclk FREQ.}}{100\text{d} * framewidth}$$

pclk FREQ.: frequency of pixel clock

< Group A >

(104)Iris control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
104	68	iris_control	0	00	00000000	RW	5	0	Iris control

register name : iris_control								
register #	bit#	name	default	**00**	default(h)	**00**	default(b)	**00000000**
104d (68h)	7	iris_en	0	iris ON/OFF 0b : disable 1b : enable				
	6	iris_mode	0	iris mode 0b : iris digital mode 1b : iris analog mode				
	5	x	0	Reserved				
	4		0					
	3		0					
	2		0					
	1		0					
	0		0					

▷ iris enable

iris enable/ disable selection

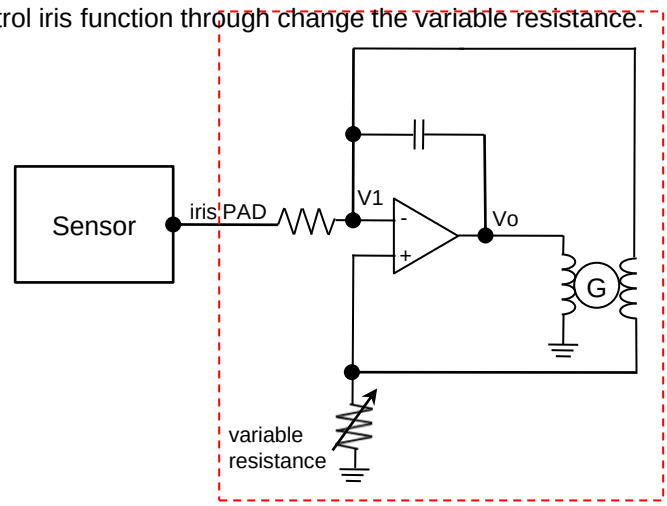
▷ iris mode

*Iris digital mode:

User can control iris function through change a iris register without change the variable resistance

*Iris analog mode :

User can control iris function through change the variable resistance.



< Group A >

< Group A >

(142~143) LED control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
142	8E	led_control1	0	00	00000000	RW	5	0	Led control

register name : led_control1								
register #	bit#	name	default	**00**	default(h)	**00**	default(b)	**00000000**
142d (8Eh)	7	ledctrl en	0	Led control 0b : disable 1b : enable				
	6	x	0	Reserved				
	5	ledctrl polarity	0	Led output polarity change 0b : disable 1b : enable				
	4	bwled en	0	Black & white mode @ led on 0b : disable 1b : enable				
	3	mirs en	0	Moving IR/AR glass switch (MIRS) control 0b : disable 1b : enable				
	2	x	0	Reserved				
	1		0					
	0	mirs polarity	0	MIRS output polarity change 0b : disable 1b : enable				

▷ ledctrl en

According to set led_control1[7] , LED control can be set as enable or disable (0b: disable, 1b: enable).

▷ bwled en

When set as led_control1[4] = '1b' & LED pad is ON, It can be selected to color mode or black&white mode.

▷ mirs en

According to set led_control1[3], Moving IR/AR glass switch (MIRS) control can be set as enable or disable (0b: disable, 1b: enable).

< Group A >

(142~143) LED control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
143	8F	led_control2	1	01	00000001	RW	5	0	Led control

register name : led_control2								
register #	bit#	name	default	**01**	default(h)	**01**	default(b)	**00000001**
143d (8Fh)	7	x	0	Reserved				
	7	x	0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2		0					
	1	x	0	Reserved				
	0	exrom_set_en	1	enable setting from external rom @ led on/off 0b: disable, 1b: enable				

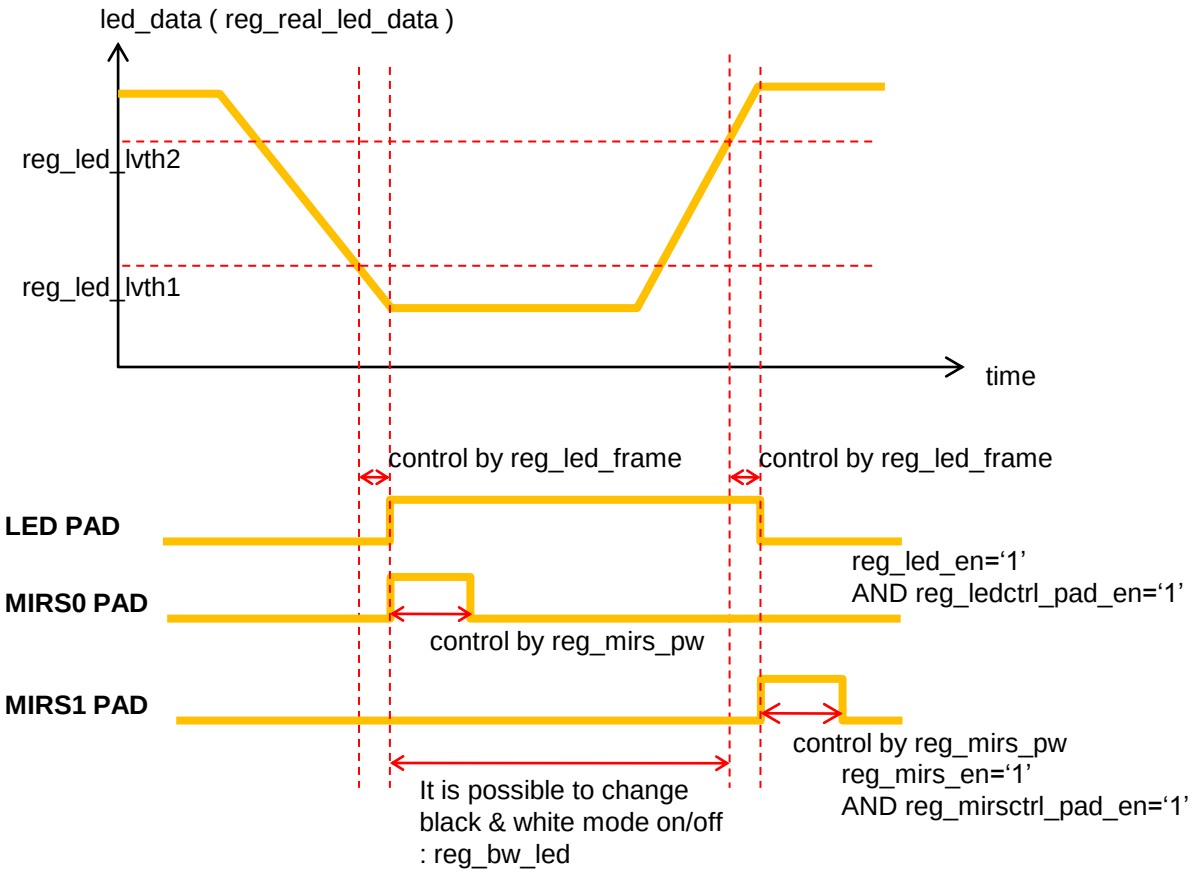
▷ **exrom_set enable**

set as led_control2[0]='1' , according to LED on and LED off ,Initial code can be set different value when using external ROM(i2c/spi)

< Group A >

(144~148) LED control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
144	90	led_lvth1	0	00	00000000	RW	5	0	Led control level th.1
145	91	led_lvth2	0	00	00000000	RW	5	0	Led control level th.2
146	92	led_frame	128	80	10000000	RW	5	0	Led frame control
147	93	mirs_pw	100	64	01100100	RW	5	0	Mirs pulse width
148	94	iris_pw	100	64	01100100	RW	5	0	Iris pulse width



< Group B >

(277) Bayer control 01

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
277	15	bayer_control_01	5	05	00000101	RW	5	0	Bayer control

register name : bayer_control_01								
register #	bit#	name	default	**5**	default(h)	**05**	default(b)	**00000101**
277d (15h)	7	x	0	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2		1					
	1	led_dsel	0	LED data selection (for 8bit) 01b : LED data[7:0] 10b : LED data[8:1] else : LED data[9:2]				
	0		1					

< Group B >

(278) Bayer control 02

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
278	16	bayer_control_02	250	FA	11111010	RW	5	0	Bayer control

register name : bayer_control_02								
register #	bit#	name	default	**250**	default(h)	**FA**	default(b)	**11111010**
278d (16h)	7	x	1	Reserved				
	6	x	1	Reserved				
	5	x	1	Reserved				
	4	x	1	Reserved				
	3	x	1	Reserved .				
	2	inv_led	0	led data inverting 0b: inverting disable 1b: inverting enable				
	1	x	1	Reserved				
	0	x	0	Reserved				

< Group B >

(416~424) Front black control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
416	A0	front_black_ref0	0	00	00000000	RW	5	0	Front black control
417	A1	front_black_ref1	0	00	00000000	RW	5	0	
418	A2	front_black_ref2	0	00	00000000	RW	5	0	
419	A3	front_black_ref3	0	00	00000000	RW	5	0	
420	A4	front_black_ref4	0	00	00000000	RW	5	0	
421	A5	front_black_ref5	0	00	00000000	RW	5	0	
422	A6	front_black_min	255	FF	11111111	RW	5	0	
423	A7	front_black_max	127	7F	01111111	RW	5	0	
424	A8	front_black	0	00	00000000	RW	6	aev	

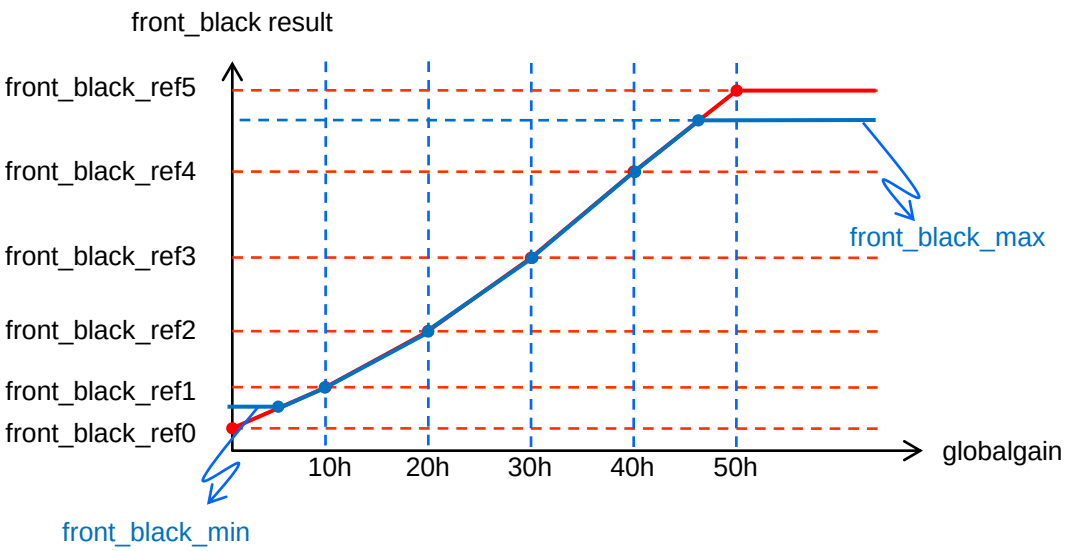
▷ ***dark_front_black***

auto_ control_3[4] ='1' *front_black_ref0~5* is fitting as below graph

auto_control_3[4]='0' then user can program the front_black manually

▶ front_black : [7] : sign bit, [6:0] : magnitude

Auto_control_3 register is located at Bank E 0x06



< Group B >

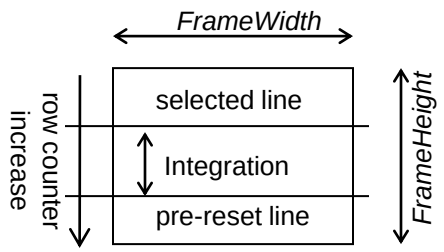
< Group B >

(444~446) Integration time.

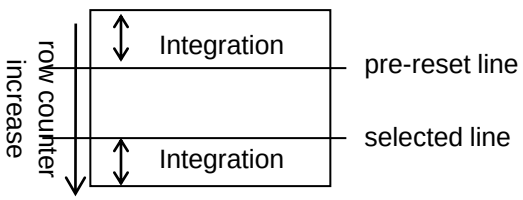
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
444	BC	inttime_h	1	01	00000001	RW	6	aev	Integration time (line)
445	BD	inttime_m	64	40	01000000	RW	6	aev	
446	BE	inttime_l	0	00	00000000	RW	6	aev	Integration time (column)

▷ integration time

There are 3 bytes of registers to control the photo-charge accumulation interval for each pixel. BCh and BEh registers indicate how many line times the integration will continue until they are all reset. BEh register further sub-divides one line time into 256 smaller intervals. Total integration time is the sum of the integral multiple and fractional parts of one line time. As the row counter value is incremented from 0 to FrameHeight, each line relevant to the row count is selected and all pixel data of that line is read out all at once. The read- out operation involves pixel reset pulses, so all pixels that are selected and read out are reset to initial states. To control exposure time, there runs another counter to select and reset a line other than the one that is selected to be read out. The space between the two lines is equal to the number of integration lines. There are two possible situations concerning the position of selected line and reset line. The 1st case is where the pre-reset counter runs ahead of read-out counter. And the other case Is just the reverse of the 1st one. The number of integration lines is different for the two cases as is shown in the left figures. Since the basic unit of integration time for PC3089N is 1/ 256 line time, it is easy to implement Auto Exposure algorithms without worrying about strong light environment where the image may change abruptly in brightness or it may even blink.



Case 1. Reset line preceding select line



Case 2. Select line preceding reset line

< Group B >

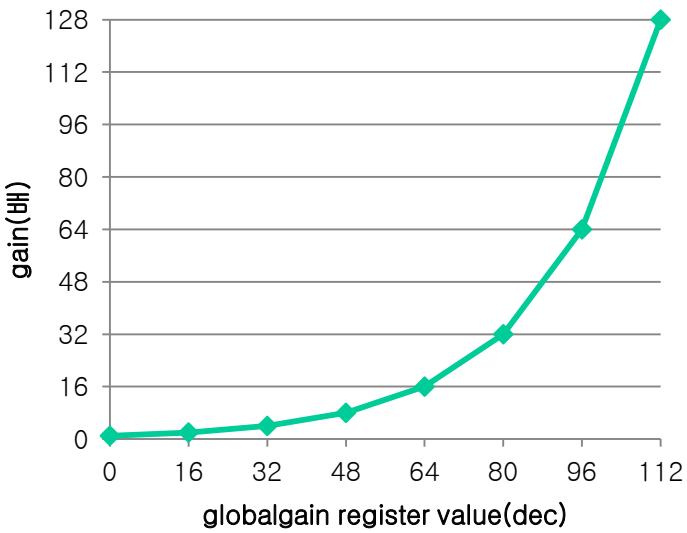
< Group B >

(447) Global gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
447	BF	globalgain	0	00	00000000	RW	6	aev	Analog gain

▷ **global gain**

GlobalGain has effect on all of R, G, and B pixel outputs. Raw R, G, B data are amplified by a common factor of GlobalGain. The relation between GlobalGain and amplification factor is shown in the picture below.



(448) Digital gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
448	C0	digitalgain	64	40	01000000	RW	6	aev	Digital gain

▷ **digital gain**

digitalgain[7:6] : Integer

digitalgain[5:0] : Fraction

(471~482, 484~491) Monitoring registers

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
471	D7	real_led_data	0	00	00000000	RO	0	0	Current CdS data

< Group C >

(518) ISP function control 2

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
518	06	isp_func_2	0	00	00000000	RW	6	aev	Isp function control

register name : isp_func_2								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
518d (06h)	7	x	0	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2	md_sleep	0	Motion detection sleep 0b : disable, 1b : enable				
	1	md_alarm	0	Motion detection alarm on screen 0b : disable, 1b : enable				
	0	md_alarm_mode	0	Motion detection alarm mode selection 0b : disable, 1b : enable				

< Group C >

(520) ISP function control 4

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
520	08	isp_func_4	0	00	00000000	RW	6	aev	Isp function control

register name : isp_func_4								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
520d (08h)	7	x	0	Reserved				
	6		0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	prvc_en	0	privacy mode enable 0b : disable 1b : enable				
	2	x	0	Reserved				
	1	md_led	0	motion led power down mode enable 0b : disable 1b : enable				
	0	x	0	Reserved				

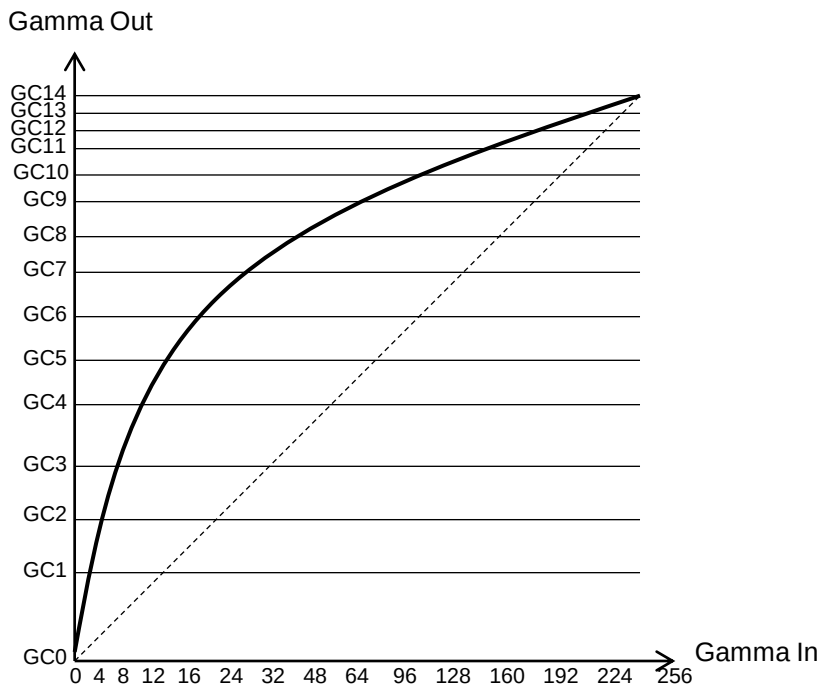
< Group C >

(573~587) Y Gamma1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
573	3D	ygm1_y0	0	00	00000000	RW	5	0	Y gamma1 coefficient
574	3E	ygm1_y1	12	0C	00001100	RW	5	0	
575	3F	ygm1_y2	32	20	00100000	RW	5	0	
576	40	ygm1_y3	47	2F	00101111	RW	5	0	
577	41	ygm1_y4	58	3A	00111010	RW	5	0	
578	42	ygm1_y5	75	4B	01001011	RW	5	0	
579	43	ygm1_y6	88	58	01011000	RW	5	0	
580	44	ygm1_y7	109	6D	01101101	RW	5	0	
581	45	ygm1_y8	127	7F	01111111	RW	5	0	
582	46	ygm1_y9	156	9C	10011100	RW	5	0	
583	47	ygm1_y10	180	B4	10110100	RW	5	0	
584	48	ygm1_y11	202	CA	11001010	RW	5	0	
585	49	ygm1_y12	221	DD	11011101	RW	5	0	
586	4A	ygm1_y13	239	EF	11101111	RW	5	0	
587	4B	ygm1_y14	255	FF	11111111	RW	5	0	

▷ Y gamma1 coefficient

Y Gamma1 Correction is applied to luminance signal which ranges from 0 to 255 to compensate non-linear characteristics of display brightness vs input brightness.



GC : Gamma coefficient

< Group C >

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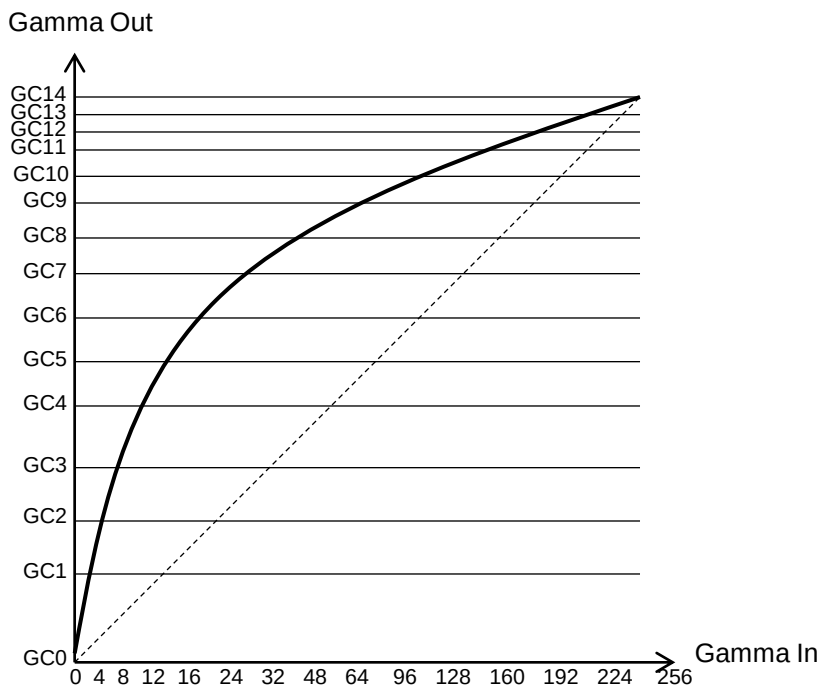
(588~602) Y Gamma2

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
588	4C	ygm2_y0	0	00	00000000	RW	5	0	Y gamma2 coefficient
589	4D	ygm2_y1	17	11	00010001	RW	5	0	
590	4E	ygm2_y2	27	1B	00011011	RW	5	0	
591	4F	ygm2_y3	35	23	00100011	RW	5	0	
592	50	ygm2_y4	42	2A	00101010	RW	5	0	
593	51	ygm2_y5	55	37	00110111	RW	5	0	
594	52	ygm2_y6	66	42	01000010	RW	5	0	
595	53	ygm2_y7	86	56	01010110	RW	5	0	
596	54	ygm2_y8	104	68	01101000	RW	5	0	
597	55	ygm2_y9	135	87	10000111	RW	5	0	
598	56	ygm2_y10	163	A3	10100011	RW	5	0	
599	57	ygm2_y11	188	BC	10111100	RW	5	0	
600	58	ygm2_y12	212	D4	11010100	RW	5	0	
601	59	ygm2_y13	234	EA	11101010	RW	5	0	
602	5A	ygm2_y14	255	FF	11111111	RW	5	0	

▷ Y gamma2 coefficient

Y Gamma2 Correction is applied to luminance signal which ranges from 0 to 255 to compensate non-linear characteristics of display brightness vs input brightness. In many cases, power function of 0.45 is used as gamma function for CRT display.

▶ Difference of Y Gamma1 and Y Gamma2 was selected by exposure. When exposure's value is increasingly high, Y Output data is affected by the Y Gamma2.



< Group C >

GC : Gamma coefficient

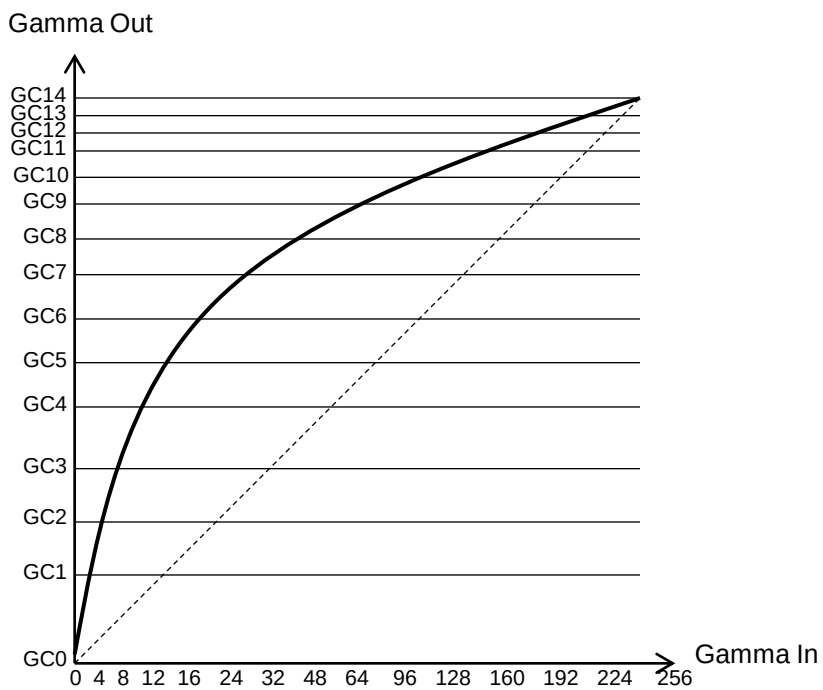
< Group C >

(603~617) RGB Gamma1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
603	5B	cgm1_y0	0	00	00000000	RW	5	0	RGB gamma1 coefficient
604	5C	cgm1_y1	15	0F	00001111	RW	5	0	
605	5D	cgm1_y2	38	26	00100110	RW	5	0	
606	5E	cgm1_y3	55	37	00110111	RW	5	0	
607	5F	cgm1_y4	67	43	01000011	RW	5	0	
608	60	cgm1_y5	84	54	01010100	RW	5	0	
609	61	cgm1_y6	98	62	01100010	RW	5	0	
610	62	cgm1_y7	119	77	01110111	RW	5	0	
611	63	cgm1_y8	136	88	10001000	RW	5	0	
612	64	cgm1_y9	164	A4	10100100	RW	5	0	
613	65	cgm1_y10	187	BB	10111011	RW	5	0	
614	66	cgm1_y11	207	CF	11001111	RW	5	0	
615	67	cgm1_y12	224	E0	11100000	RW	5	0	
616	68	cgm1_y13	241	F1	11110001	RW	5	0	
617	69	cgm1_y14	255	FF	11111111	RW	5	0	

▷ RGB gamma1 coefficient

RGB Gamma1 Correction is applied to chrominance signal which ranges from 0 to 255 to compensate non-linear characteristics of display color vs input color.



GC : Gamma coefficient

< Group C >

< Group C >

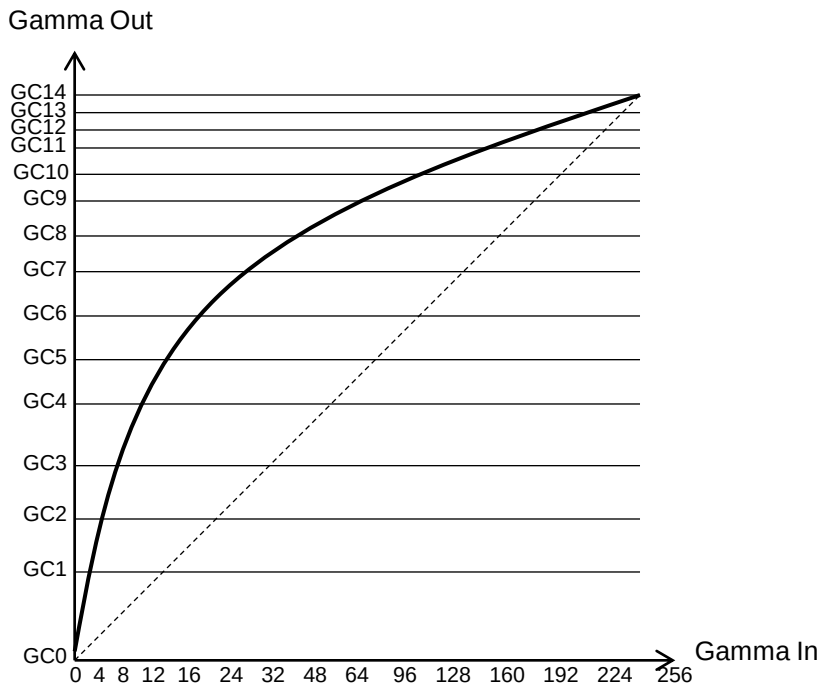
(618~632) RGB Gamma2

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
618	6A	cgm2_y0	0	00	00000000	RW	5	0	RGB gamma2 coefficient
619	6B	cgm2_y1	7	07	00000111	RW	5	0	
620	6C	cgm2_y2	13	0D	00001101	RW	5	0	
621	6D	cgm2_y3	19	13	00010011	RW	5	0	
622	6E	cgm2_y4	24	18	00011000	RW	5	0	
623	6F	cgm2_y5	34	22	00100010	RW	5	0	
624	70	cgm2_y6	44	2C	00101100	RW	5	0	
625	71	cgm2_y7	62	3E	00111110	RW	5	0	
626	72	cgm2_y8	79	4F	01001111	RW	5	0	
627	73	cgm2_y9	111	6F	01101111	RW	5	0	
628	74	cgm2_y10	142	8E	10001110	RW	5	0	
629	75	cgm2_y11	172	AC	10101100	RW	5	0	
630	76	cgm2_y12	200	C8	11001000	RW	5	0	
631	77	cgm2_y13	228	E4	11100100	RW	5	0	
632	78	cgm2_y14	255	FF	11111111	RW	5	0	

▷ RGB gamma2 coefficient

RGB Gamma2 Correction is applied to chrominance signal which ranges from 0 to 255 to compensate non-linear characteristics of display color vs input color.

▶ Difference of RGB Gamma1 and RGB Gamma2 was selected by exposure. When exposure's value is increasingly high, RGB Output data is affected by the Y Gamma2.



GC : Gamma coefficient

(653~655) Y weight & Y max & Y min

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
653	8D	y_weight	64	40	01000000	RW	6	aev	Y weight

(657~664) Y contrast and Y brightness

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
657	91	ycontrast_ref0	64	40	01000000	RW	5	0	Y contrast fitting control
658	92	ycontrast_ref1	64	40	01000000	RW	5	0	
659	93	ycontrast_ref2	64	40	01000000	RW	5	0	
660	94	ycontrast	64	40	01000000	RW	6	aev	
661	95	ybrightness_ref0	240	F0	00000000	RW	5	0	Y brightness fitting control
662	96	ybrightness_ref1	0	00	00000000	RW	5	0	
663	97	ybrightness_ref2	0	00	00000000	RW	5	0	
664	98	ybrightness	0	00	00000000	RW	6	aev	

▷ ***Dark_ycontrast & dark_ybrightness***

Ycontrast & Ybrightness darkness control registers.

filter_control1[5] = '0b', then user can program ycontrast/ybrightness manually.

filter_control1[5] = '1b', ycontrast/ybrightness is fitting as below graph.

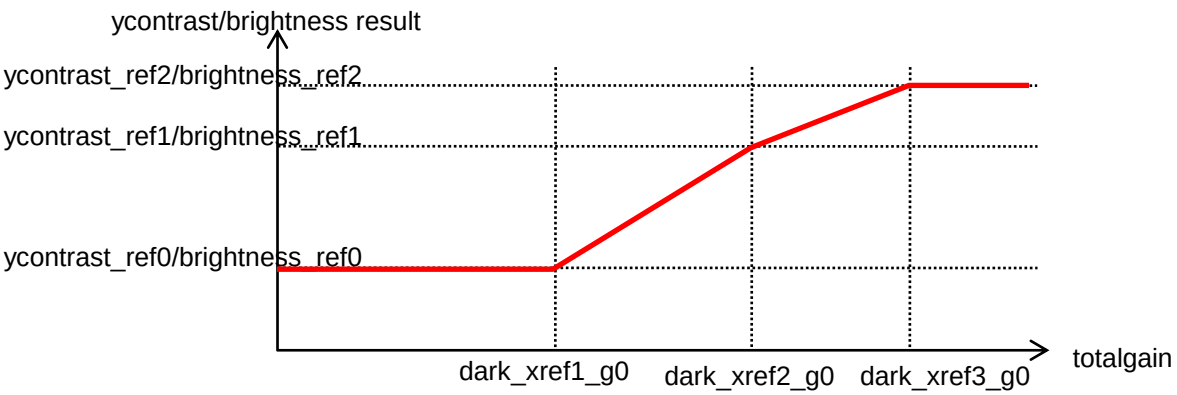
"filter_control1" register address is Group E 0x82

★ ***dark_ycontrast0/1/2 conditions*** *are givens as*

00h ≤ *ycontrast* ≤ FF

★ ***dark_ybrightness0/1/2 conditions*** *are givens as*

-128d ≤ *ybrightness* ≤ 127d



< Group C >

(672~682) Privacy

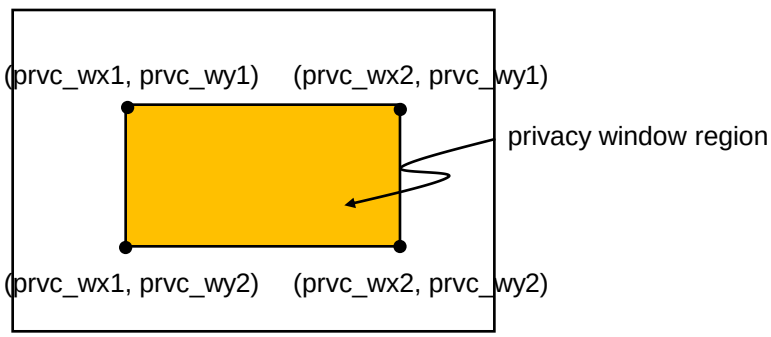
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
672	A0	prvc_wx1_h	0	00	xxxxxx00	RW	5	0	Privacy window size control
673	A1	prvc_wx1_l	1	01	00000001	RW	5	0	
674	A2	prvc_wx2_h	2	02	xxxxxx10	RW	5	0	
675	A3	prvc_wx2_l	128	80	10000000	RW	5	0	
676	A4	prvc_wy1_h	0	00	xxxxxx00	RW	5	0	
677	A5	prvc_wy1_l	1	01	00000001	RW	5	0	
678	A6	prvc_wy2_h	0	00	xxxxxx00	RW	5	0	
679	A7	prvc_wy2_l	240	F0	11110000	RW	5	0	
680	A8	prvc_y	0	00	00000000	RW	5	0	YCbCr of privacy window
681	A9	prvc_cb	128	80	10000000	RW	5	0	
682	AA	prvc_cr	128	80	10000000	RW	5	0	

▷ ***prvc_wx1/wx2, prvc_wy1/wy2***

Privacy window control registers.

▷ ***prvc_y/cb/cr***

Region of privacy window change the color.



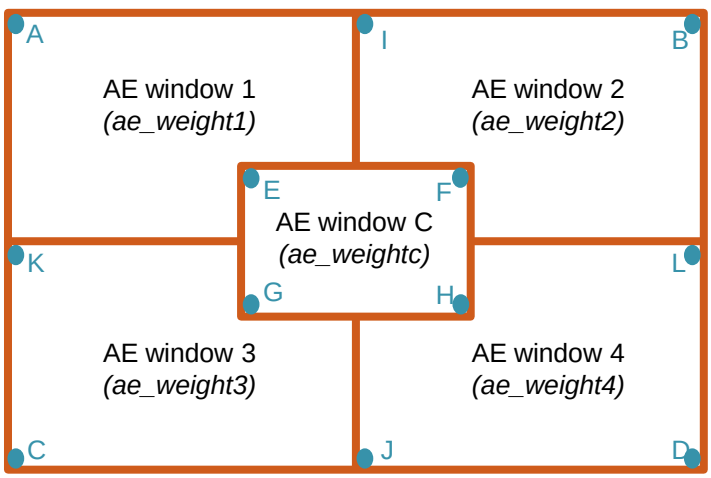
< Group C >

(691~710) Auto exposure window control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
691	B3	ae_fwx1_h	0	00	xxxxxx00	RW	5	0	AE full window X start position
692	B4	ae_fwx1_l	1	01	00000001	RW	5	0	
693	B5	ae_fwx2_h	2	02	xxxxxx10	RW	5	0	AE full window X stop position
694	B6	ae_fwx2_l	208	D0	11010000	RW	5	0	
695	B7	ae_fwy1_h	0	00	xxxxxx00	RW	5	0	AE full window Y start position
696	B8	ae_fwy1_l	1	01	00000001	RW	5	0	
697	B9	ae_fwy2_h	1	01	xxxxxx01	RW	5	0	AE full window Y stop position
698	BA	ae_fwy2_l	224	E0	11100000	RW	5	0	
699	BB	ae_cwx1_h	0	00	xxxxxx00	RW	5	0	AE center window X start position
700	BC	ae_cwx1_l	241	F1	11110001	RW	5	0	
701	BD	ae_cwx2_h	1	01	xxxxxx01	RW	5	0	AE center window X stop position
702	BE	ae_cwx2_l	224	E0	11100000	RW	5	0	
703	BF	ae_cwy1_h	0	00	xxxxxx00	RW	5	0	AE center window Y start position
704	C0	ae_cwy1_l	161	A1	10100001	RW	5	0	
705	C1	ae_cwy2_h	1	01	xxxxxx01	RW	5	0	AE center window Y stop position
706	C2	ae_cwy2_l	64	40	01000000	RW	5	0	
707	C3	ae_xaxis_h	1	01	xxxxxx01	RW	5	0	AE window X axis
708	C4	ae_xaxis_l	105	69	01101001	RW	5	0	
709	C5	ae_yaxis_h	0	00	xxxxxx00	RW	5	0	AE window Y axis
710	C6	ae_yaxis_l	241	F1	11110001	RW	5	0	

▷ AE window control

AE window control registers



A : *(ae_fwx1, ae_fwy1)*
B : *(ae_fwx2, ae_fwy1)*
C : *(ae_fwx1, ae_fwy2)*
D : *(ae_fwx2, ae_fwy2)*
E : *(ae_cwx1, ae_cwy1)*
F : *(ae_cwx2, ae_cwy1)*
G : *(ae_cwx1, ae_cwy2)*
H : *(ae_cwx2, ae_cwy2)*
I : *(ae_xaxis, ae_fwy1)*
J : *(ae_xaxis, ae_fwy2)*
K : *(ae_fwx1, ae_yaxis)*
L : *(ae_fwx2, ae_yaxis)*

< Group C >

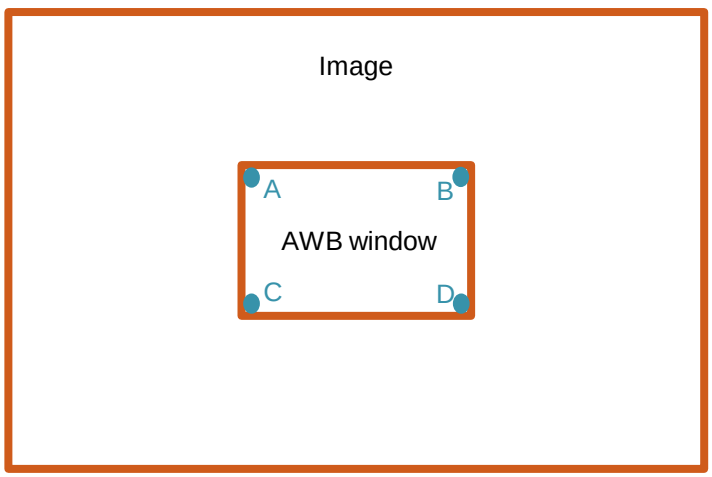
< Group C >

(711~718) AWB window control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
711	C7	awb_wx1_h	0	00	xxxxxx00	RW	5	0	AWB window X start position
712	C8	awb_wx1_l	1	01	00000001	RW	5	0	
713	C9	awb_wx2_h	2	02	xxxxxx10	RW	5	0	AWB window X stop position
714	CA	awb_wx2_l	208	D0	11010000	RW	5	0	
715	CB	awb_wy1_h	0	00	xxxxxx00	RW	5	0	AWB window Y start position
716	CC	awb_wy1_l	1	01	00000001	RW	5	0	
717	CD	awb_wy2_h	1	01	xxxxxx01	RW	5	0	AWB window Y stop position
718	CE	awb_wy2_l	224	E0	11100000	RW	5	0	

▷ *AWB window control*

AWB window control registers.



A : *(awb_wx1, awb_wy1)*
B : *(awb_wx2, awb_wy1)*
C : *(awb_wx1, awb_wy2)*
D : *(awb_wx2, awb_wy2)*

< Group C >

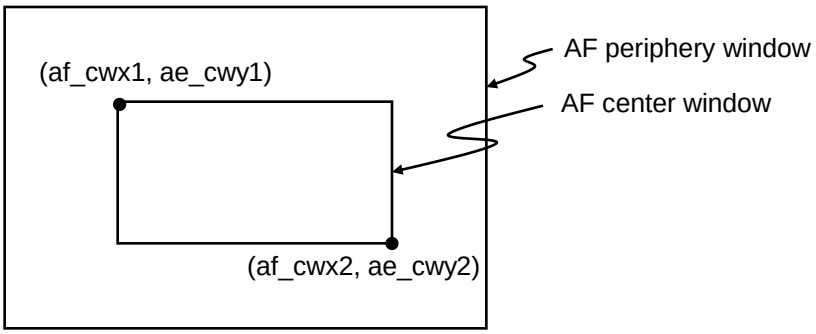
(728~737) Auto focus control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
728	D8	af_cwx1_h	0	00	xxxxxx00	RW	5	0	AF center window X start position
729	D9	af_cwx1_l	241	F1	11110001	RW	5	0	
730	DA	af_cwx2_h	1	01	xxxxxx01	RW	5	0	AF center window X stop position
731	DB	af_cwx2_l	224	E0	11100000	RW	5	0	
732	DC	af_cwy1_h	0	00	xxxxxx00	RW	5	0	AF center window Y start position
733	DD	af_cwy1_l	161	A1	10100001	RW	5	0	
734	DE	af_cwy2_h	1	01	xxxxxx01	RW	5	0	AF center window Y stop position
735	DF	af_cwy2_l	64	40	01000000	RW	5	0	
736	E0	af_cweight	8	08	xxx01000	RW	5	0	AF weight center
737	E1	af_edge_th	0	00	x0000000	RW	5	0	AF edge TH

▷ af_cwx1/x2/y1/y2

AF window control registers.

default value : U ➔ wire-strapping register



▷ af_cweight

Control to the weight of AF center.

▷ af_edge_th

Control to the threshold of AF edge.

< Group C >

(739~747) Motion detection threshold

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
739	E3	md_yth1	64	40	01000000	RW	5	0	Y threshold1 for motion detection
740	E4	md_yth2	64	40	01000000	RW	5	0	Y threshold2 for motion detection
741	E5	md_yth3	64	40	01000000	RW	5	0	Y threshold3 for motion detection
742	E6	md_yth4	64	40	01000000	RW	5	0	Y threshold4 for motion detection
743	E7	md_diff1	64	40	01000000	RW	5	0	Difference1 for motion detection
744	E8	md_diff2	64	40	01000000	RW	5	0	Difference2 for motion detection
745	E9	md_diff3	64	40	01000000	RW	5	0	Difference3 for motion detection
746	EA	md_diff4	64	40	01000000	RW	5	0	Difference4 for motion detection
747	EB	md_interval	8	08	00001000	RW	5	0	Intervals of frames used for motion detection

▷ ***md_yth1/2/3/4***

Threshold of Y (luminance) mean difference between current and previous frames at the same section.

▷ ***md_diff1/2/3/4***

Difference between entire current and previous frame's brightness means.

▷ ***md_interval***

Define frame interval for motion detection.

▷ ***md_interval***

Define frame interval for motion detection.

md_yth1 *md_diff1*	*md_yth2* *md_diff2*
md_yth3 *md_diff3*	*md_yth4* *md_diff4*

▶ PC3089N is assorted with forth area of motion detection and it can control motion's threshold

< Group C >

(748~765) Motion detection & alarm

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
748	EC	md_alarm_y	0	00	00000000	RW	5	0	YCbCr for Motion detection alarm
749	ED	md_alarm_cb	128	80	10000000	RW	5	0	
750	EE	md_alarm_cr	128	80	10000000	RW	5	0	
751	EF	md_alarmnumb	4	04	00000100	RW	5	0	Number of Motion detection alarm
752	F0	md_alarm_xlw	4	04	00000100	RW	5	0	X width of motion detection alarm
753	F1	md_alarm_ylw	4	04	00000100	RW	5	0	Y width of motion detection alarm
754	F2	md_alarmdur_h	0	00	00000000	RW	5	0	Period of motion detection alarm
755	F3	md_alarmdur_l	60	3C	00111100	RW	5	0	
756	F4	md_sleepdur_h	2	02	00000010	RW	5	0	Motion detection sleep
757	F5	md_sleepdur_l	58	3A	00111010	RW	5	0	
758	F6	md_section7	0	00	00000000	RW	5	0	Image section 7 for motion detection
759	F7	md_section6	0	00	00000000	RW	5	0	Image section 6 for motion detection
760	F8	md_section5	0	00	00000000	RW	5	0	Image section 5 for motion detection
761	F9	md_section4	0	00	00000000	RW	5	0	Image section 4 for motion detection
762	FA	md_section3	0	00	00000000	RW	5	0	Image section 3 for motion detection
763	FB	md_section2	0	00	00000000	RW	5	0	Image section 2 for motion detection
764	FC	md_section1	0	00	00000000	RW	5	0	Image section 1 for motion detection
765	FD	md_section0	0	00	00000000	RW	5	0	Image section 0 for motion detection

▷ **md_alarm_y/cb/cr**

Alarm of motion detection change the color.

▷ **md_alarmnumb**

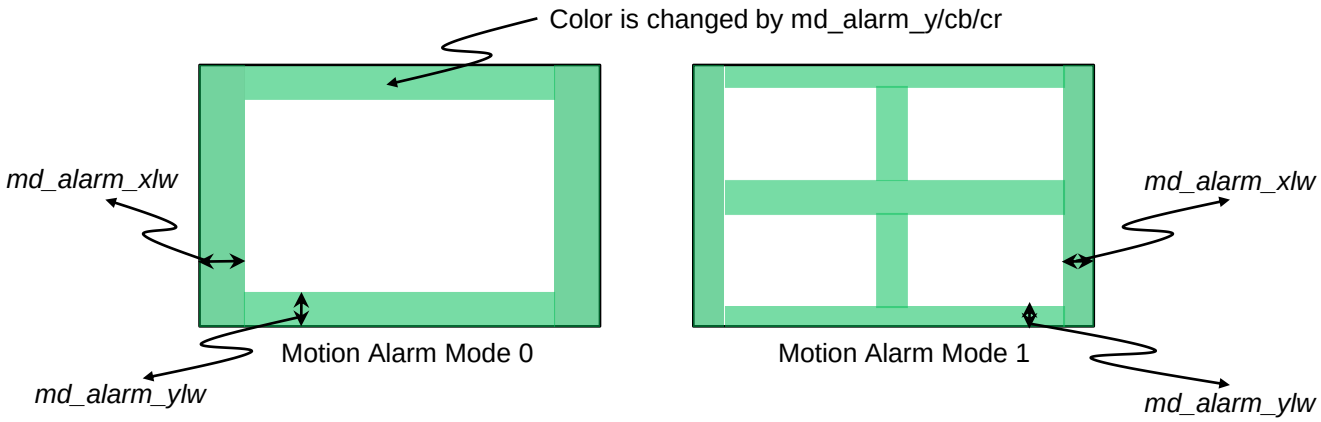
Control the number of motion detection alarm.

▷ **md_alarm_xlw**

Control the width of X's direction.

▷ **md_alarm_ylw**

Control the width of Y's direction.



▶ By the motion alarm mode showed with the upper 2 picture and according to fixed period, motion alarm blink.

< Group C >

▷ md_alarmdur_h/l

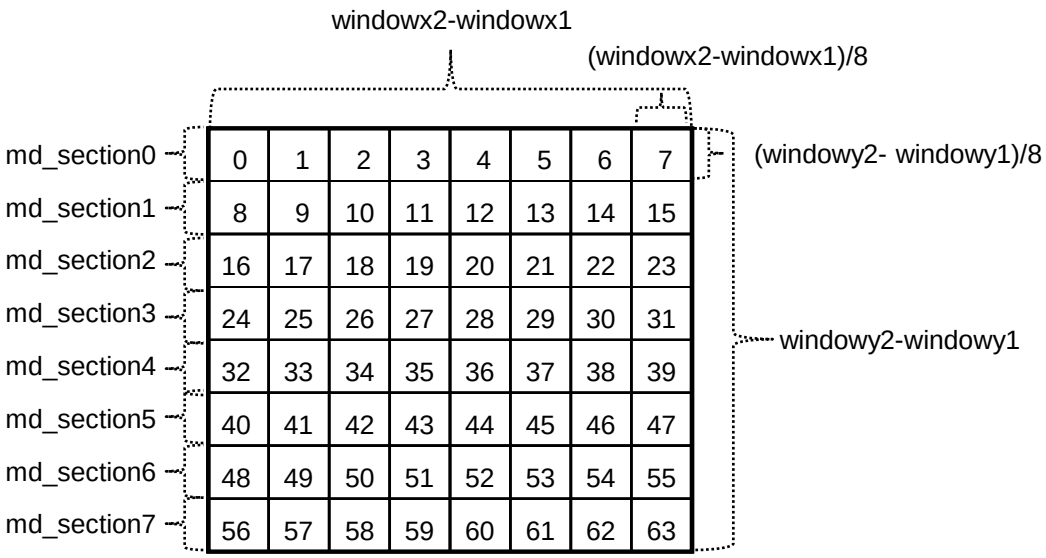
Control the flickering speed of motion alarm.

▷ md_sleepdur_h/l

When image don't have the motion during fixed time, control the power of DAC.

▷ md_section7/6/5/4/3/2/1/0

Masks of 64 sections on one frame.



▶ Register Tables (Detailed) : Group D

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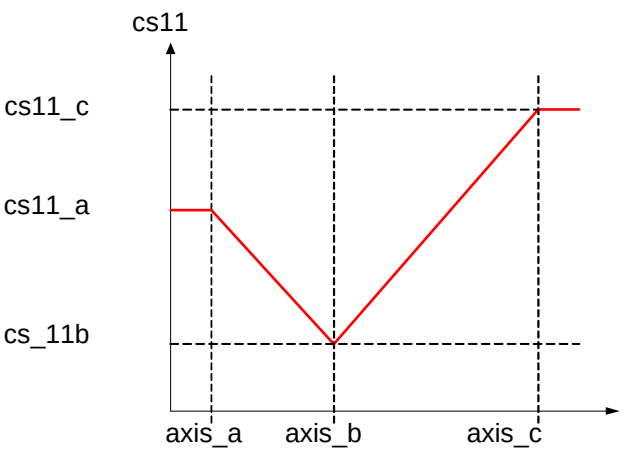
(772~793) Lens gain & CS matrix fitting reference

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
772	04	cs11_a	56	38	00111000	RW	5	0	Color saturation matrix fitting reference
773	05	cs12_a	28	1C	00011100	RW	5	0	
774	06	cs21_a	130	82	10000010	RW	5	0	
775	07	cs22_a	44	2C	00101100	RW	5	0	
776	08	cs11_b	35	23	00100011	RW	5	0	
777	09	cs12_b	0	00	00000000	RW	5	0	
778	0A	cs21_b	0	00	00000000	RW	5	0	
779	0B	cs22_b	39	27	00100111	RW	5	0	
780	0C	cs11_c	39	27	00100111	RW	5	0	
781	0D	cs12_c	130	82	10000010	RW	5	0	
782	0E	cs21_c	2	02	00000010	RW	5	0	
783	0F	cs22_c	36	24	00100100	RW	5	0	
784	10	lens_gainr_a	6	06	00000110	RW	5	0	Lens gain fitting reference
785	11	lens_gainb_a	0	00	00000000	RW	5	0	
786	12	lens_gainr_b	2	02	00000010	RW	5	0	
787	13	lens_gainb_b	0	00	00000000	RW	5	0	
788	14	lens_gainr_c	2	02	00000010	RW	5	0	
789	15	lens_gainb_c	0	00	00000000	RW	5	0	
790	16	axis_a	48	30	00110000	RW	5	0	CS matrix / lens gain fitting reference
791	17	axis_b	80	50	01010000	RW	5	0	
792	18	axis_c	94	5E	01011110	RW	5	0	
793	19	user_cs	56	38	00111000	RW	5	0	User CS gain

▷ CS matrix fitting reference & Lens gain fitting reference



- * Calculation method of cs12, cs21 and cs22 are same as calculation method of cs11.

* bit define of cs11_a/b/c
  [7] : sign
  [6:5] : magnitude of integer
  [4:0] : magnitude of fraction

wb_rgain
or
wb_bgain

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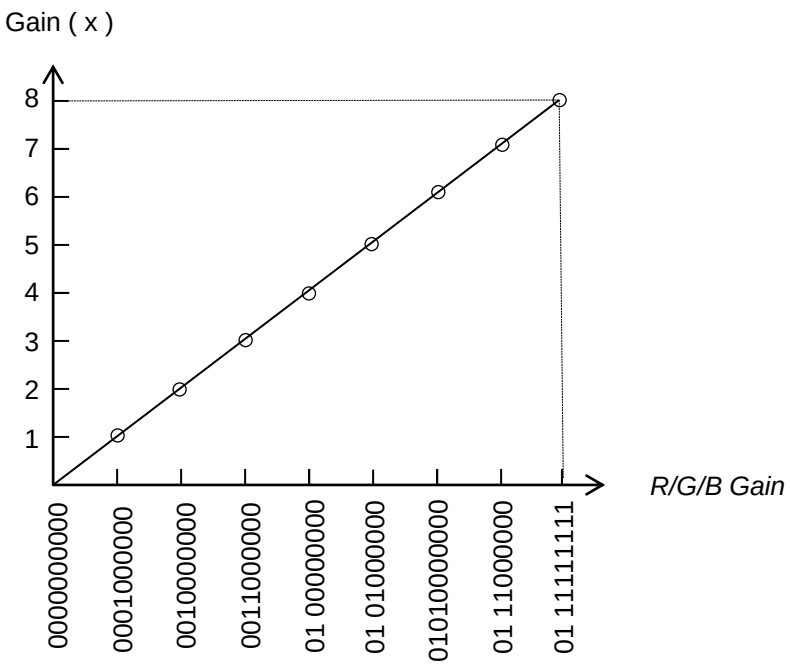
(795~800) Normalized white balance gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
795	1B	wb_rgain_h	0	00	00000000	RW	6	aev	Normalized white balance gain
796	1C	wb_rgain_l	93	5D	01011101	RW	6	aev	
797	1D	wb_ggain_h	0	00	00000000	RW	6	aev	
798	1E	wb_ggain_l	64	40	01000000	RW	6	aev	
799	1F	wb_bgain_h	0	00	00000000	RW	6	aev	
800	20	wb_bgain_l	94	5E	01011110	RW	6	aev	

▷ wb_r/g/bgain

When operating awb_normalization function, If one of wb_gain is lower than 40h, that is replace 40h, and other wb gain is calculated that other wb gain is multiply same weight



gain_h[1:0] : integer

gain_l[7:6] : Integer

gain_l[5:0] : Fraction

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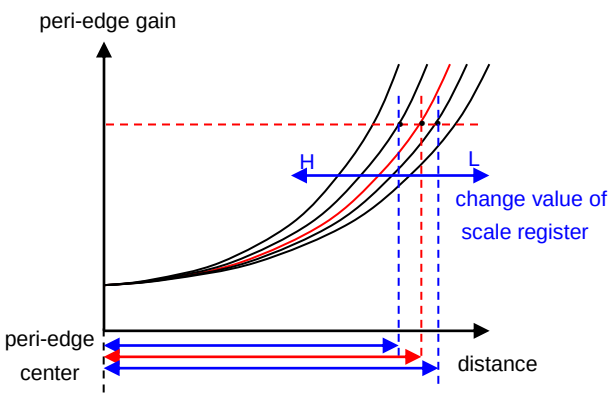
(861~865) Peripheral edge

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
861	5D	periedge_gain	0	00	00000000	RW	5	0	Peripheral edge gain

▷ **periedge_gain**

When user use a wide-angle lens , you know that peripheral edge become blurred. By using the periedge_gain, peripheral edges are enhanced.



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(869~876) ec_pth / ec_mth dark filter

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
869	65	dark_ec_pth0	4	04	00000100	RW	5	0	Dark edge clamp plus threshold filter control
870	66	dark_ec_pth1	4	04	00000100	RW	5	0	
871	67	dark_ec_pth2	4	04	00000100	RW	5	0	
872	68	dark_ec_pth	4	04	00000100	RW	6	aev	
873	69	dark_ec_mth0	4	04	00000100	RW	5	0	Dark edge clamp minus threshold filter control
874	6A	dark_ec_mth1	32	20	00100000	RW	5	0	
875	6B	dark_ec_mth2	48	30	00110000	RW	5	0	
876	6C	dark_ec_mth	4	04	00000100	RW	6	aev	

▷ ec_pth / ec_mth dark filter

edge clamp threshold registers.

filter_control1[7] = '0b', then user can program dark_ec_pth / dark_ec_mth manually.

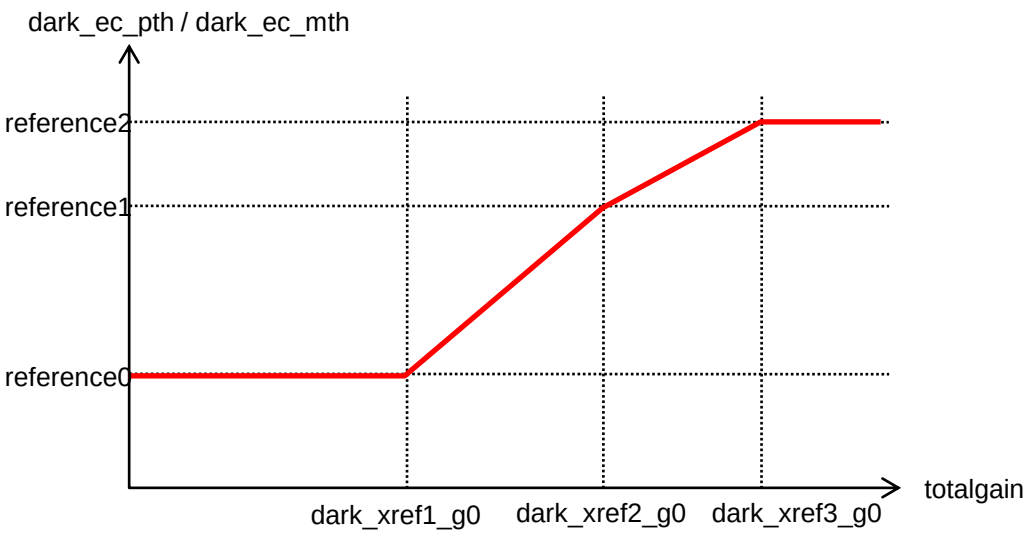
filter_control1[7] = '1b', dark_ec_pth / dark_ec_mth is fitting as below graph.

"filter_control1" register address is Group E 0x82

★ ***dark_ec_pth / dark_ec_mth conditions*** are given as

00h ≤ dark_ec_pth0 ≤ dark_ec_pth1 ≤ dark_ec_pth2 ≤ FFh

00h ≤ dark_ec_mth0 ≤ dark_ec_mth1 ≤ dark_ec_mth2 ≤ FFh



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(887~890) de-color dark filter

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
887	77	dark_dc0	0	00	00000000	RW	5	0	de-color dark filter
888	78	dark_dc1	8	08	00001000	RW	5	0	
889	79	dark_dc2	16	10	00010000	RW	5	0	
890	7A	dark_dc	0	00	00000000	RW	6	aev	

▷ **de-color dark filter**

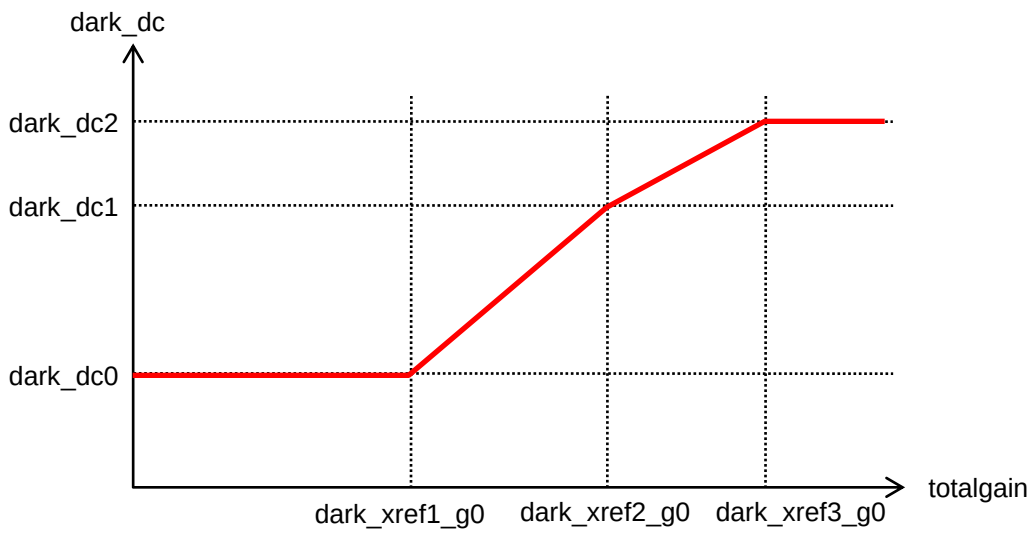
Color correction control registers.

filter_control1[7] = '0b', then user can program *dark_dc* manually.

filter_control1[7] = '1b', dark_dc is fitting as below graph.

"filter_control1" register address is Group E 0x82

★ ***dark_dc conditions : 00h ≤ dark_dc0 ≤ dark_dc1 ≤ dark_dc2 ≤ 3Fh***



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(901~916) Monitoring register

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
901	85	motion_monitor7	0	00	00000000	RO	0	0	Current motion detection indicator
902	86	motion_monitor6	0	00	00000000	RO	0	0	
903	87	motion_monitor5	0	00	00000000	RO	0	0	
904	88	motion_monitor4	0	00	00000000	RO	0	0	
905	89	motion_monitor3	0	00	00000000	RO	0	0	
906	8A	motion_monitor2	0	00	00000000	RO	0	0	
907	8B	motion_monitor1	0	00	00000000	RO	0	0	
908	8C	motion_monitor0	0	00	00000000	RO	0	0	
909	8D	af_edge_sum3	0	00	00000000	RO	0	0	Edge data for auto focus
910	8E	af_edge_sum2	0	00	00000000	RO	0	0	
911	8F	af_edge_sum1	0	00	00000000	RO	0	0	
912	90	af_edge_sum0	0	00	00000000	RO	0	0	

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(1009~1012) edge gain low frequency

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1009	F1	edge_gain_lf0	48	30	00110000	RW	5	0	edge gain lf dark filter fiting
1010	F2	edge_gain_lf1	48	30	00110000	RW	5	0	
1011	F3	edge_gain_lf2	48	30	00110000	RW	5	0	
1012	F4	edge_gain_lf	48	30	00110000	RW	6	aev	

▷ ***edge_gain_lf***

edge_gain_lf control registers.

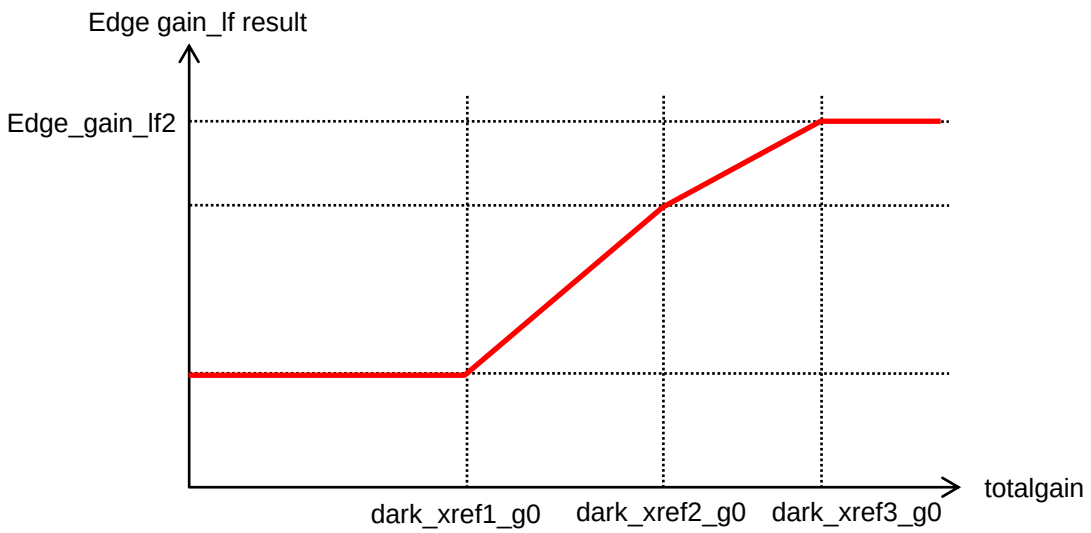
filter_control1[7] = '0b' : then user can program *edge_gain_lf* manually.

filter_control1[7] = '1b' : *edge_gain_lf* is fitting as below graph.

"filter_control1" register address is Group E 0x82

★ ***edge_gain_lf conditions*** are given as

00h ≤ *edge_gain_lf* ≤ FFh



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▶ Register Tables (Detailed) : Group E

(1028) Auto_control_1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1028	04	auto_control_1	152	98	10011000	RW	6	autov	Auto control

register name : auto_control_1								
register #	bit#	name	default	**152**	default(h)	**98**	default(b)	**10011000**
1028d (04h)	7	x	1	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	x	1	Reserved				
	3	x	1	Reserved				
	2	AWB mode	0	White blance mode selection 0b : auto mode, 1b : manual mode				
	1	exposure mode	0	Exposure mode selection 00b : auto mode 01b : manual mode (exposure write) 10b : manual mode (ext_inttime, ext_glbgain write) 11b : manual mode (inttime, globalgain write)				
	0		0					

▷ AWB mode

When auto_control_1[2] is '1', auto white balance dose not operation and you can write white balance gain(Reg. D-1Bh~20h). Please set disable, before writing white balance gain.

▷ AE mode

PC3089N provides auto exposure mode and 3 type of manual exposure mode.
User can select auto exposure mode by writing auto_control_1[1:0].

▶ auto_control_1[1:0] = 00b (auto exposure mode)

When auto_control_1[1:0] is 00h, integration time, global gain and digital gain are calculated by auto exposure block. Refer to auto exposure reference register(Reg. E-12h~20h).

▶ auto_control_1[1:0] = 01b (manual exposure mode1)

When auto_control_1[1:0] is 01h, integration time, global gain and digital by exposure register(Reg. E-27~2Ah).

▶ auto_control_1[1:0] = 10b (manual exposure mode2)

When auto_control_1[1:0] is 10h, you can control integration time, global gain and digital gain by external integration time and external linear global gain register(Reg. E-22h~26h).

▶ auto_control_1[1:0] = 11b (manual exposure mode3)

When auto_control_1[1:0] is 11h, you can write integration time, global gain register.
Refer to Reg. B_BCh~C0h

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(1042~1056) AE reference registers

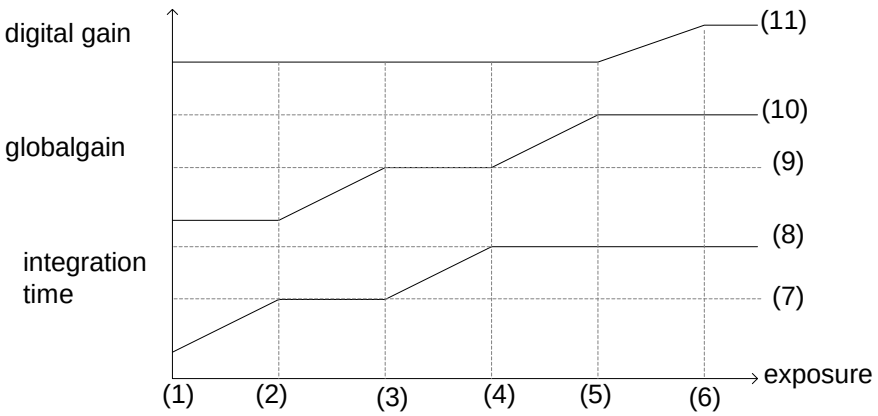
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1042	12	expfrmh_h	2	02	00000010	RW	5	0	AE reference
1043	13	expfrmh_l	u	u	uuuuuuuu	RW	5	0	
1044	14	midfrmheight_h	2	02	00000010	RW	5	0	
1045	15	midfrmheight_l	u	u	uuuuuuuu	RW	5	0	
1046	16	maxfrmheight_h	2	02	00000010	RW	5	0	
1047	17	maxfrmheight_l	u	u	uuuuuuuu	RW	5	0	
1048	18	minexp_h	0	00	00000000	RW	5	0	
1049	19	minexp_m	0	00	00000000	RW	5	0	
1050	1A	minexp_l	40	28	00101000	RW	5	0	
1051	1B	midexp_t	2	02	00000010	RW	5	0	
1052	1C	midexp_h	71	47	01000111	RW	5	0	
1053	1D	midexp_m	224	E0	11100000	RW	5	0	
1054	1E	maxexp_t	4	04	00000100	RW	5	0	
1055	1F	maxexp_h	143	8F	10001111	RW	5	0	
1056	20	maxexp_m	192	C0	11000000	RW	5	0	

▷ AE reference registers

Auto Exposure reference control registers.

When auto_control_1[1:0] is 00b or 01b, integration time, globalgain and digitalgain are calculated using AE reference registers .

default value : U ➔ wire-strapping register



(1) minimum exposure
(2) frame height for exposure
(3) mid frame height for exposure
(4) max frame height for exposure
(5) mid exposure
(6) max exposure
(7) mid integration time = (2)
(8) max integration time = (4)/(9)
(9) mid globalgain = (3)/(2)
(10) max globalgain =(5)/(8)
(11) max digital gain = (6)/{ (10)*(8) }

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(1058~1062) Manual integration time and linear globalgain for external AE mode

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1058	22	ext_inttime_h	0	00	00000000	RW	6	autov	Manual integration time @ external AE mode
1059	23	ext_inttime_m	128	80	10000000	RW	6	autov	
1060	24	ext_inttime_l	0	00	00000000	RW	6	autov	
1061	25	ext_glbg_h	1	01	00000001	RW	6	autov	Manual analog gain @ external AE mode
1062	26	ext_glbg_l	0	00	00000000	RW	6	autov	

▷ ext_inttime

When auto_control_1[1:0] is 10b, user can control integration time by writing external integration time registers. Ext_inttime_h and ext_inttime_m are line of external integration time. Ext_inttime_l is column of external integration time.

▷ ext_globalgain

When auto_control_1[1:0] is 10b, user can control globalgain by writing external linear globalgain registers.

Set auto_control_1[1:0] to 10b, before writing external integration time.

(1063~1066) Exposure

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1063	27	exposure_t	0	00	00000000	RW	6	autov	Exposure
1064	28	exposure_h	1	01	00000001	RW	6	autov	
1065	29	exposure_m	64	40	01000000	RW	6	autov	
1066	2A	exposure_l	0	00	00000000	RW	6	autov	

▷ exposure

When auto_control_1[1:0] is 00b, exposure registers are calculated by auto exposure block. Exposure registers are used in calculating integration time, globalgain and digital gain.

When auto_control_1[1:0] is 01b, user can write exposure registers.

Set auto_control_1[1:0] to 01b, before writing exposure registers.

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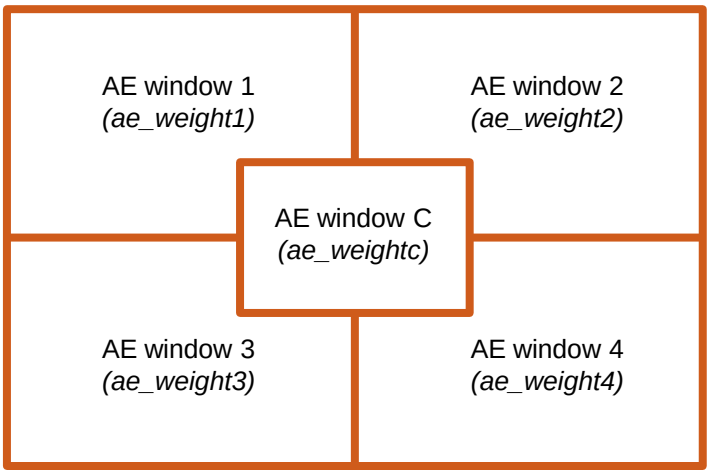
(1072~1076) AE weight

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1072	30	ae_weight1	8	08	xx001000	RW	5	0	AE weight peripheral
1073	31	ae_weight2	8	08	xx001000	RW	5	0	
1074	32	ae_weight3	8	08	xx001000	RW	5	0	
1075	33	ae_weight4	8	08	xx001000	RW	5	0	
1076	34	ae_weightc	8	08	xx001000	RW	5	0	AE weight center

▷ ***ae_weight1/2/3/4/c***

AE data weight for BLC(back light compensation)



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(1077~1082) Y mean reference & Y mean

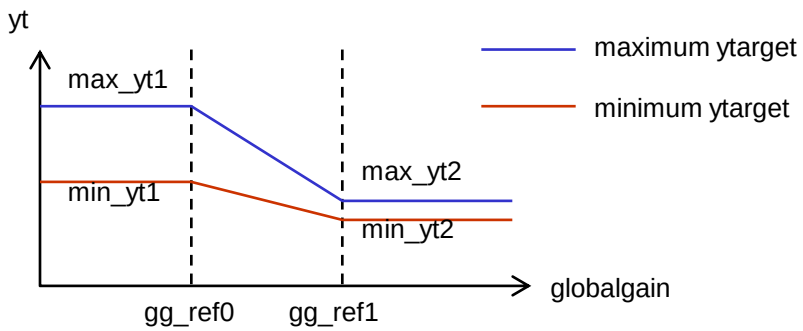
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1081	39	ymean_h	0	00	00000000	RW	5	0	Y mean
1082	3A	ymean_l	128	80	10000000	RW	5	0	

(1083~1086) Min/Max Y target reference

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1083	3B	max_yt1	152	98	10011000	RW	6	autov	Min / max ytarget control reference
1084	3C	max_yt2	80	50	01010000	RW	6	autov	
1085	3D	min_yt1	152	98	10011000	RW	6	autov	
1086	3E	min_yt2	80	50	01010000	RW	6	autov	

▷ min/max_yt1/2

User can program dynamic y_target with these registers. Dynamic y_target means that y_target can be changed to match current brightness automatically.



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(1089~1095) Y target reference & Y target

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1095	47	user_wyt	128	80	10000000	RW	6	autov	User weight Y target

▷ ***user_wyt***

Ytarget = (ytarget x *user_wyt*) / 128d

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(1096~1097) AE speed

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1096	48	ae_up_speed	4	04	00000100	RW	6	autov	AE upside speed
1097	49	ae_down_speed	4	04	00000100	RW	6	autov	AE downside speed

▷ **ae_up_speed & ae_down_speed**

yt ≥ ym : AE_speed = *ae_up_speed*

yt < ym : AE_speed = *ae_down_speed*

If ae_up_speed and ae_down_speed have high value,
auto exposure speed will be faster. However, high ae_up_speed and ae_down_speed value may cause AE oscillation.

(1098~1099) AE lock range & auto flag

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1098	4A	ae_lock	5	05	00010000	RW	6	autov	AE lock range

▷ **ae_lock**

AE lock range control register.
Setting range of ae_lock is 00h to FFh.
If ae_lock has low value, auto exposure lock range will be smaller.
However, small value of ae_lock may cause AE oscillation.

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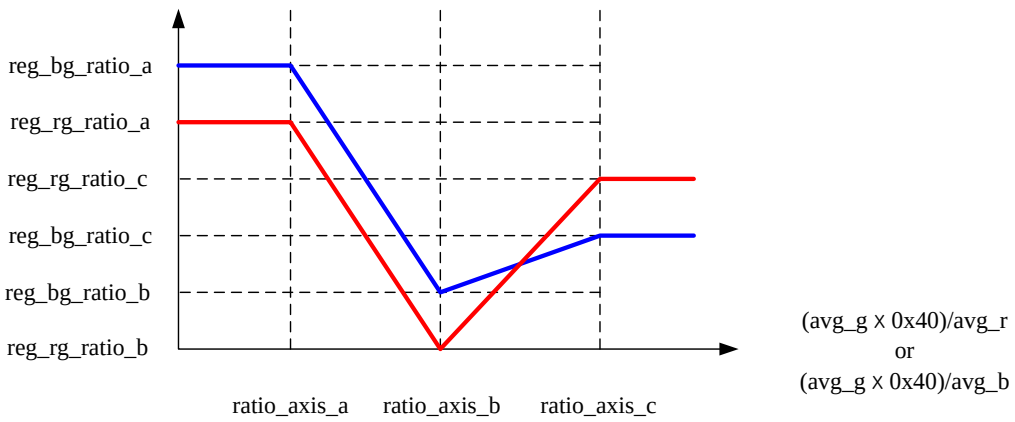
(1128~1138) rg/bg ratio reference & rg/bg ratio

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1128	68	rg_ratio_a	128	80	10000000	RW	5	0	Target awb ratio fitting reference
1129	69	bg_ratio_a	128	80	10000000	RW	5	0	
1130	6A	rg_ratio_b	128	80	10000000	RW	5	0	
1131	6B	bg_ratio_b	128	80	10000000	RW	5	0	
1132	6C	rg_ratio_c	128	80	10000000	RW	5	0	
1133	6D	bg_ratio_c	128	80	10000000	RW	5	0	
1134	6E	ratio_axis_a	48	30	00110000	RW	5	0	
1135	6F	ratio_axis_b	80	50	01010000	RW	5	0	
1136	70	ratio_axis_c	94	5E	01011110	RW	5	0	
1137	71	awb_rgratio	128	80	10000000	RW	5	0	AWB RG ratio control
1138	72	awb_bgratio	128	80	10000000	RW	5	0	AWB BG ratio control

▷ RG/BG_ratio_a/b/c

Target AWB ratio fitting reference

: These registers are used for deciding AWB target. It's possible to enable or disable these registers by controlling auto_control_3[7].



User can change the value of X-axis by using auto_cotnrol_3[6].

'1b': avg_gx0x40/avg_r

'0b': avg_gx0x40/avg_b

Caution) ratio_axis_a < ratio_axis_b < ratio_axis_c

▷ AWB_RG/BGratio

AWB target control registers

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(1139~1140) AWB lock range & speed

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1139	73	awb_lock	6	06	00000110	RW	5	0	AWB lock range
1140	74	awb_speed	4	04	00000100	RW	5	0	AWB speed

▷ AWB_lock

AE lock range control register.

Setting range of awb_lock is 00h to FFh. If awb_lock has low value, awb lock range will be smaller. However, small value of awb_lock may cause AWB oscillation.

▷ AWB_speed

If awb_speed have high value, AWB speed will be faster.

However, high awb speed value may cause AE oscillation.

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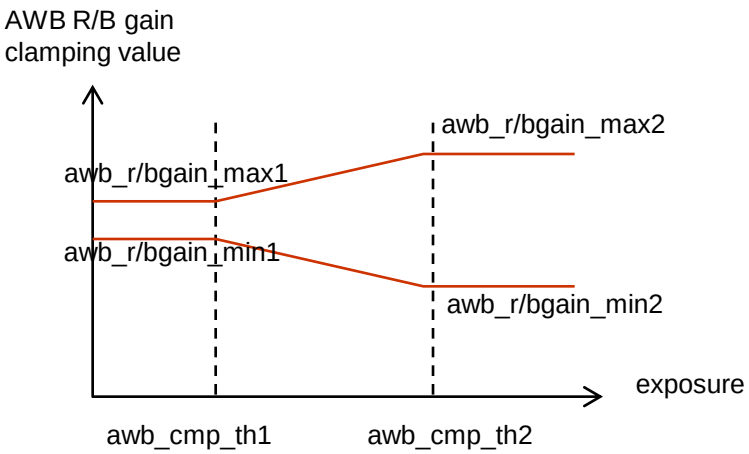
(1141~1152) AWB gain min/max clamping reference

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1141	75	awb_rgain_min1	0	00	00000000	RW	5	0	AWB gain clamping fitting control
1142	76	awb_rgain_min2	0	00	00000000	RW	5	0	
1143	77	awb_rgain_max1	255	FF	11111111	RW	5	0	
1144	78	awb_rgain_max2	255	FF	11111111	RW	5	0	
1145	79	awb_bgain_min1	0	00	00000000	RW	5	0	
1146	7A	awb_bgain_min2	0	00	00000000	RW	5	0	
1147	7B	awb_bgain_max1	255	FF	11111111	RW	5	0	
1148	7C	awb_bgain_max2	255	FF	11111111	RW	5	0	
1149	7D	awb_cmp_th1_h	0	00	00000000	RW	5	0	
1150	7E	awb_cmp_th1_m	128	80	10000000	RW	5	0	
1151	7F	awb_cmp_th2_h	1	01	00000001	RW	5	0	
1152	80	awb_cmp_th2_m	0	00	00000000	RW	5	0	

▷ ***AWB_r/bgain_min/max***

AWB gain min/max clamping



00h < *awb_r/bgain_min1* < *awb_r/bgain_max1* < FFh

00h < *awb_r/bgain_min2* < *awb_r/bgain_max2* < FFh

minexp < *awb_cmp_th1* < *awb_cmp_th2* < *maxexp*

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(1154) filter_ctrl_1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1154	82	filter_ctrl_1	240	F0	11110000	RW	6	autov	filter control

register name : filter_ctrl_1								
register #	bit#	name	default	**224**	default(h)	**E0**	default(b)	**11100000**
1154d (82h)	7	dark filter fitting	1	dark filter fitting enable 0b : disable 1b : enable				
	6	x	1	reserved				
	5	ycontrast/brightness fi tting	1	ycontrast, ybrightness fitting enable 0b : disable 1b : enable				
	4	x	1	reserved				
	3	x	0	reserved				
	2	x	0	reserved				
	1	x	0	reserved				
	0	x	0	reserved				

▷ dark filter fitting

Dark filter fitting enable / disable

▷ ycontrast/brightness fitting

Ycontrast/brightnsee fitting enable / disable

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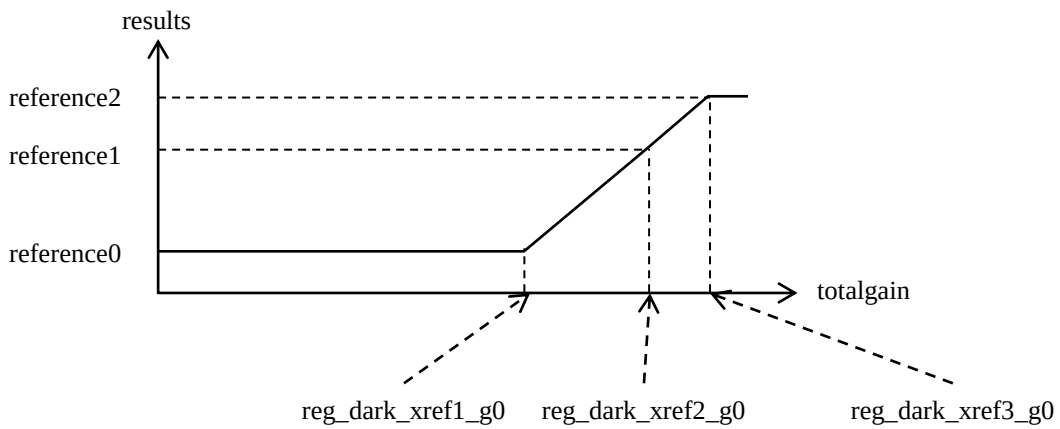
(1165~1178) Dark filter horizontal axis control register

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1165	8D	dark_xref1_g0_h	0	00	00000000	RW	5	0	Dark filter x-axis reference
1166	8E	dark_xref1_g0_l	6	06	00000110	RW	5	0	
1167	8F	dark_xref2_g0_h	0	00	00000000	RW	5	0	
1168	90	dark_xref2_g0_l	16	10	00010000	RW	5	0	
1169	91	dark_xref3_g0_h	0	00	00000000	RW	5	0	
1170	92	dark_xref3_g0_l	32	20	00100000	RW	5	0	

▷ **dark_xref1/2/3_g0**

dark_filter horizontal axis fitting registers.

dark_xref1/2/3_g0 register is reference point for dark filter.



(1179~1180) Total gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1179	9B	totalgain_h	0	00	00000000	RW	6	autov	Total gain
1180	9C	totalgain_l	1	01	00000001	RW	6	autov	

▷ **totalgain**

Dark_filter reference control registers.

▶ Register Tables (Detailed) : Group F

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(1284)Parking Guide Line control 0

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1284	04	pg_control0	9	09	00001001	RW	6	aev	Embedded parking guide line control

register name : pg_control0								
register #	bit#	name	default	**9**	default(h)	**09**	default(b)	**00001001**
1284d (04h)	7	x	0	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	pg_hlight	0	all pg hlight enable				
	3	x	1	Reserved				
	2	pg_rm	0	remove left side of PG				
	1		0	remove right side of PG				
	0	pg_enable	1	PG enable 0b: disable 1b: enable				

▷ pg_hlight

Total high light zone can be enable/disable at embedded parking guide line.

▷ pg_rm

pg_control0[2] : removing left side of PG ➔ '1b' : removing, '0b' : don't removing

pg_control0[1] : removing right side of PG ➔ '1b' : removing, '0b' : don't removing

▷ pg_enable

PG is enable /disable by pg_control0[0] register bit.

Embedded parking guide line can be show that OSD layer3 does not use by external SPI ROM.

If user use to OSD layer 3 by external SPI ROM, pg_control[0] should be set as '0b'.

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(1285)Embedded Parking Guide Line control 1

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1285	05	pg_control1	0	00	00000000	RW	6	aev	Embedded parking guide line control

register name : pg_control1								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
1285d (05h)	7	x	0	Reserved				
	6	pg_cl_pal	0	pg center line palette number				
	5		0					
	4		0					
	3	pg_cl_type	0	pg_center line type 0b: dashed line 1b: solid line				
	2	pg_cl_en	0	pg center line enable				
	1	x	0	Reserved				
	0	x	0	Reserved				

▷ pg_cl_pal

Palette number of parking guide center line

▷ pg_cl_type

It is can be control that type of parking guide center line.

‘0b’ : dashed line

‘1b’ : solid line

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(1286)Embedded Parking Guide Line control 2

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1286	06	pg_control2	0	00	00000000	RW	6	aev	Embedded parking guide line control

register name : pg_control2								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
1286d (06h)	7	x	0	Reserved				
	6	pg_ch_pal	0	pg character palette number				
	5		0					
	4		0					
	3	x	0	Reserved				
	2	x	0	Reserved				
	1	x	0	Reserved				
	0	pg_ch_enable	0	pg character enable				

▷ ***pg_ch_pal***

Palette number of Parking guideline character

.

▷ ***pg_ch_enable***

PG_character is enable /disable by pg_control1[0] register bit.

Embedded PG character can be show that OSD layer2 does not use by external SPI ROM.

If user use to OSD layer 2 by external SPI ROM, pg_control1[0] should be set as '0b'.

(1288~1320)Embedded Parking Guide Line

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#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1288	08	pg_yt	127	7F	01111111	RW	6	aev	Embedded parking guide line control
1289	09	pg_y1	115	73	01110011	RW	6	aev	
1290	0A	pg_y2	2	02	00000010	RW	6	aev	
1291	0B	pg_y3	8	08	00001000	RW	6	aev	
1292	0C	pg_y4	15	0F	00001111	RW	6	aev	
1293	0D	pg_y5	25	19	00011001	RW	6	aev	
1294	0E	pg_y6	37	25	00100101	RW	6	aev	
1295	0F	pg_y7	40	28	00101000	RW	6	aev	
1296	10	pg_y8	56	38	00111000	RW	6	aev	
1297	11	pg_y9	78	4E	01001110	RW	6	aev	
1298	12	pg_y10	82	52	01010010	RW	6	aev	
1299	13	pg_a	143	8F	10001111	RW	6	aev	
1300	14	pg_b	100	64	01100100	RW	6	aev	
1301	15	pg_c	191	BF	10111111	RW	6	aev	
1302	16	pg_d	7	07	00000111	RW	6	aev	
1303	17	pg_e	12	0C	00001100	RW	6	aev	
1304	18	pg_f	21	15	00010101	RW	6	aev	
1305	19	pg_line1	33	21	00100001	RW	6	aev	
1306	1A	pg_line2	35	23	00100011	RW	6	aev	
1307	1B	pg_line3	36	24	00100100	RW	6	aev	
1308	1C	pg_line4	70	46	01000110	RW	6	aev	
1309	1D	pg_line5	72	48	01001000	RW	6	aev	
1310	1E	pg_line6	66	42	01000010	RW	6	aev	
1311	1F	pg_line7	75	4B	01001011	RW	6	aev	
1312	20	pg_line8	113	71	01110001	RW	6	aev	
1313	21	pg_line9	99	63	01100011	RW	6	aev	
1314	22	pg_line10	116	74	01110100	RW	6	aev	
1315	23	pg_center_h	1	01	xxxxxx01	RW	6	aev	
1316	24	pg_center_l	104	68	01101000	RW	6	aev	
1317	25	pg_l_type_h	1	01	xxxxxx01	RW	6	aev	
1318	26	pg_l_type_l	33	21	00100001	RW	6	aev	
1319	27	pg_hl_en_h	0	00	xxxxxx00	RW	6	aev	
1320	28	pg_hl_en_l	0	00	00000000	RW	6	aev	

▷ pg_yt

The boundary of straight line and a curve

▷ pg_y1/10

The start position of 10 points

▷ pg_a

X-axis Start point, X-axis value = 2x(pg_a), Min=01h

▷ pg_b

The slope of embedded parking guide line.

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(1288~1320)Embedded Parking Guide Line

▷ ***pg_c***

The weight of slope.

▷ ***pg_d***

Embedded parking guide line Width (Min : 04h)

▷ ***pg_e***

Embedded parking guide line width weight.

▷ ***pg_f***

long line width

▷ ***pg_line1/10***

The information decision of each dot line
pg_line1~10 (7): line type ➔ '0': short line width
'1': long line width
pg_line1~10 [6:5]: palette color information of line
➔ palette number 0~3
pg_line1~10 [4:0]: height of each line.

▷ ***pg_center***

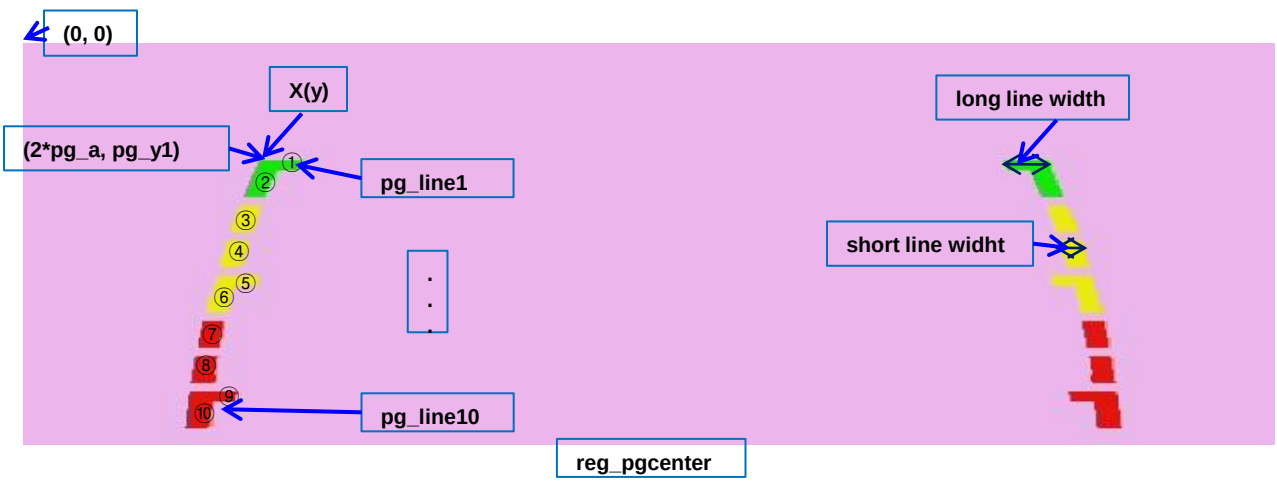
It defines the center position of embedded parking guide line.

▷ ***pg_l_type***

Set to type of each line의
'0': width type1(reg_d + e(y-y1) , '1': width type2(reg_f*width1)

▷ ***pg_hl_en***

Highlight zone of each line enable/disable



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(1288~1320)Embedded Parking Guide Line

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▷ Embedded parking guide line default value

The following table is value for the NTSC & PAL PG position.
(Condition: VSYNC pad(strap_master_en) = '1')

Register name	NTSC mode	PAL_mode
pg_yt	7F	7F
pg_y1	73	8C
pg_y2	02	02
pg_y3	08	08
pg_y4	0F	11
pg_y5	19	1C
pg_y6	25	2A
pg_y7	28	2D
pg_y8	38	40
pg_y9	4E	59
pg_y10	52	5D
pg_a	8F	8F
pg_b	64	5F
pg_c	BF	BF
pg_d	07	07
pg_e	0C	0A
pg_f	15	15
pg_line1	21	21
pg_line2	23	23
pg_line3	24	26
pg_line4	46	47
pg_line5	48	4A
pg_line6	42	42
pg_line7	4B	4E
pg_line8	71	74
pg_line9	63	63
pg_line10	74	7A

▷ Embedded Parking Guide Line condition.

1. It can be expression to 10 dot line.(max)
2. Each dotted line is the y coordinate of the starting point should be lower than the top line.
   pg_y1+line1_height(pg_line1[4:0]+1) < pg_y2 … line9_height(pg_line9[4:0]+1) < pg_y10
3. PG image from top to bottom, should be increasingly wider.
4. The left and right line should be separated more than the minimum 8pixel line.

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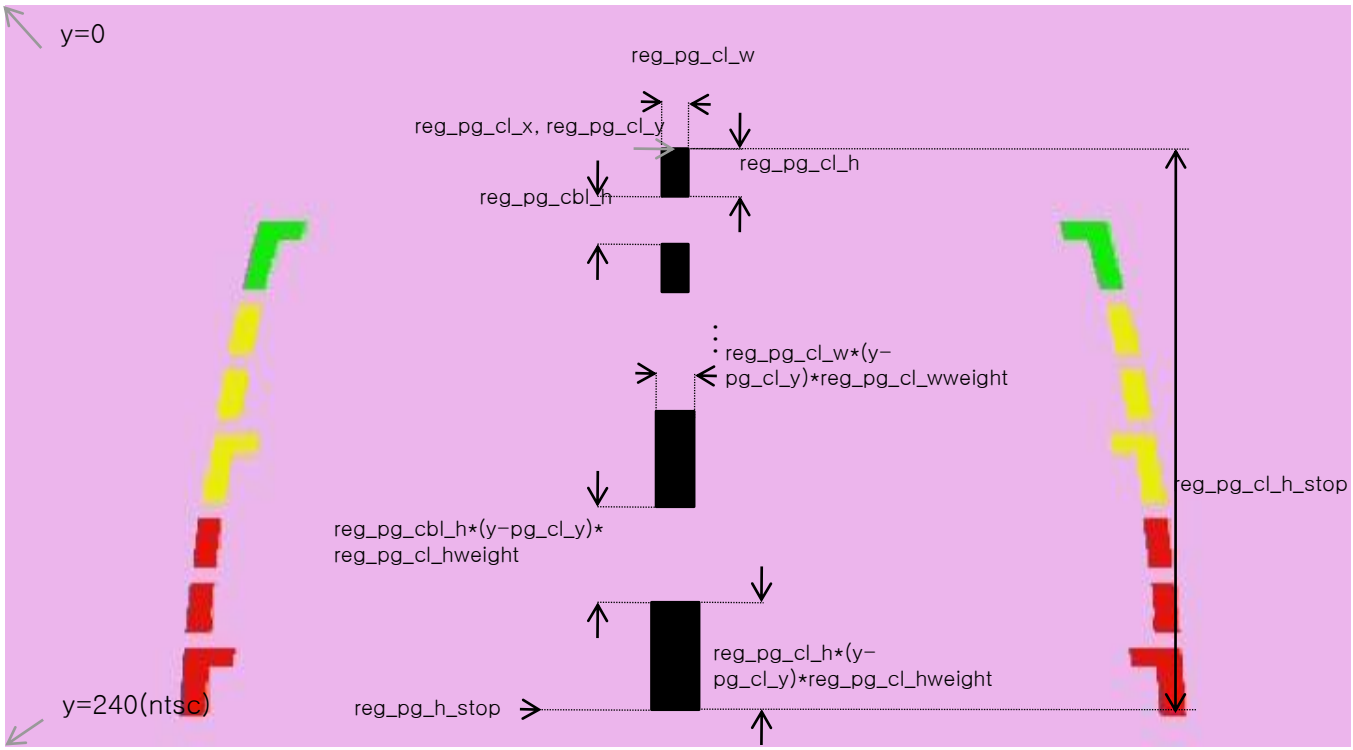
(1321~1330)Embedded Parking Guide Center Line

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1321	29	pg_cl_x_h	0	00	xxxxxx00	RW	5	0	Embedded parking guide line control
1322	2A	pg_cl_x_l	0	00	00000000	RW	5	0	
1323	2B	pg_cl_y	0	00	00000000	RW	5	0	
1324	2C	pg_cl_h_stop_h	0	00	xxxxxxx0	RW	5	0	
1325	2D	pg_cl_h_stop_l	0	00	00000000	RW	5	0	
1326	2E	pg_cl_w	0	00	00000000	RW	5	0	
1327	2F	pg_cl_hght	0	00	00000000	RW	5	0	
1328	30	pg_cbl_hght	0	00	00000000	RW	5	0	
1329	31	pg_cl_wweight	0	00	00000000	RW	5	0	
1330	32	pg_cl_hweight	0	00	00000000	RW	5	0	



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(1332~1363)Embedded PG character

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1332	34	pg_string0_x_h	1	01	xxxxxxx1	RW	5	0	Embedded PG string position
1333	35	pg_string0_x_l	255	FF	11111111	RW	5	0	
1334	36	pg_string1_x_h	1	01	xxxxxxx1	RW	5	0	
1335	37	pg_string1_x_l	255	FF	11111111	RW	5	0	
1336	38	pg_string2_x_h	1	01	xxxxxxx1	RW	5	0	
1337	39	pg_string2_x_l	255	FF	11111111	RW	5	0	
1338	3A	pg_string3_x_h	1	01	xxxxxxx1	RW	5	0	
1339	3B	pg_string3_x_l	255	FF	11111111	RW	5	0	
1340	3C	pg_string4_x_h	1	01	xxxxxxx1	RW	5	0	
1341	3D	pg_string4_x_l	255	FF	11111111	RW	5	0	
1342	3E	pg_string5_x_h	1	01	xxxxxxx1	RW	5	0	
1343	3F	pg_string5_x_l	255	FF	11111111	RW	5	0	
1344	40	pg_string6_x_h	1	01	xxxxxxx1	RW	5	0	
1345	41	pg_string6_x_l	255	FF	11111111	RW	5	0	
1346	42	pg_string7_x_h	1	01	xxxxxxx1	RW	5	0	
1347	43	pg_string7_x_l	255	FF	11111111	RW	5	0	
1348	44	pg_string0_y_h	1	01	xxxxxxx1	RW	5	0	
1349	45	pg_string0_y_l	255	FF	11111111	RW	5	0	
1350	46	pg_string1_y_h	1	01	xxxxxxx1	RW	5	0	
1351	47	pg_string1_y_l	255	FF	11111111	RW	5	0	
1352	48	pg_string2_y_h	1	01	xxxxxxx1	RW	5	0	
1353	49	pg_string2_y_l	255	FF	11111111	RW	5	0	
1354	4A	pg_string3_y_h	1	01	xxxxxxx1	RW	5	0	
1355	4B	pg_string3_y_l	255	FF	11111111	RW	5	0	
1356	4C	pg_string4_y_h	1	01	xxxxxxx1	RW	5	0	
1357	4D	pg_string4_y_l	255	FF	11111111	RW	5	0	
1358	4E	pg_string5_y_h	1	01	xxxxxxx1	RW	5	0	
1359	4F	pg_string5_y_l	255	FF	11111111	RW	5	0	
1360	50	pg_string6_y_h	1	01	xxxxxxx1	RW	5	0	
1361	51	pg_string6_y_l	255	FF	11111111	RW	5	0	
1362	52	pg_string7_y_h	1	01	xxxxxxx1	RW	5	0	
1363	53	pg_string7_y_l	255	FF	11111111	RW	5	0	

▷ Embedded PG character position

Embedded PG string position

It is supported to max. 8 string with 4 character package

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(1364~1379) Embedded PG character

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1364	54	pg_string0_ch0	0	00	xxxx0000	RW	5	0	Embedded PG character selection in strings
1365	55	pg_string0_ch2	0	00	xxxx0000	RW	5	0	
1366	56	pg_string1_ch0	0	00	xxxx0000	RW	5	0	
1367	57	pg_string1_ch2	0	00	xxxx0000	RW	5	0	
1368	58	pg_string2_ch0	0	00	xxxx0000	RW	5	0	
1369	59	pg_string2_ch2	0	00	xxxx0000	RW	5	0	
1370	5A	pg_string3_ch0	0	00	xxxx0000	RW	5	0	
1371	5B	pg_string3_ch2	0	00	xxxx0000	RW	5	0	
1372	5C	pg_string4_ch0	0	00	xxxx0000	RW	5	0	
1373	5D	pg_string4_ch2	0	00	xxxx0000	RW	5	0	
1374	5E	pg_string5_ch0	0	00	xxxx0000	RW	5	0	
1375	5F	pg_string5_ch2	0	00	xxxx0000	RW	5	0	
1376	60	pg_string6_ch0	0	00	xxxx0000	RW	5	0	
1377	61	pg_string6_ch2	0	00	xxxx0000	RW	5	0	
1378	62	pg_string7_ch0	0	00	xxxx0000	RW	5	0	
1379	63	pg_string7_ch2	0	00	xxxx0000	RW	5	0	

▷ ***selecting Embedded PG character***

Embedded PG character selection in strings
Ch1/ch3 : '.(dot)/m' → fixed character
Ch0/ch2 : '0 ~ 9' → available

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(1435~1436) OSD blink control

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1435	9B	blink_frame	0	00	00000000	RW	5	0	OSD blink control
1436	9C	blink_control	0	00	xxxx0000	RW	5	0	

▷ OSD blink control

blink_frame speed control.

blink_control[3] : OSD laye3 blink enable

blink_control[2] : OSD layer2 blink enable

blink_control[1] : OSD layer1 blink enable

blink_control[0] : OSD layer0 blink enable

(1437) OSD boundary

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1437	9D	spi_osd_bndry	0	00	00000000	RW	5	0	OSD boundary

▷ OSD boundary

Boundary thickness control.

spi_osd_bndry[7:6] : OSD layer3 boundary

spi_osd_bndry[5:4] : OSD layer2 boundary

spi_osd_bndry[3:2] : OSD layer1 boundary

spi_osd_bndry[1:0] : OSD layer0 boundary

OSD layer0 boundary = 0d : no boundary

OSD layer0 boundary = 1d : 1pixel boundary

OSD layer0 boundary = 2d : 2pixel boundary

OSD layer0 boundary = 3d : 3pixel boundary

(OSD layer1/2/3 is also same)

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(1474~1483)SW comp

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1474	C2	sw_comp1_h	0	00	00000000	RW	5	0	Switch comparing for Embedded OSD control
1475	C3	sw_comp1_l	31	1F	00011111	RW	5	0	
1476	C4	sw_comp2_h	0	00	00000000	RW	5	0	
1477	C5	sw_comp2_l	30	1E	00011110	RW	5	0	
1478	C6	sw_comp3_h	0	00	00000000	RW	5	0	
1479	C7	sw_comp3_l	28	1C	00011100	RW	5	0	
1480	C8	sw_comp4_h	0	00	00000000	RW	5	0	
1481	C9	sw_comp4_l	24	18	00011000	RW	5	0	
1482	CA	sw_comp5_h	0	00	00000000	RW	5	0	
1483	CB	sw_comp5_l	16	10	00010000	RW	5	0	

▷ sw_comp

sw_comp1~5 is value of five direction key, sw_comp1~5 is matching center, right, left, up, down in regular sequence

sw_comp1_l~5_l(5bit of LSB) is using for ADC of OSDC PAD, that is matching OSDC PAD voltage as like below.

OSDC PAD voltage=0*AVDD : “11111”
OSDC PAD voltage=1/5AVDD : “11110”
OSDC PAD voltage=2/5AVDD : “11100”
OSDC PAD voltage=3/5AVDD : “11000”
OSDC PAD voltage=4/5AVDD : “10000”

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(1516) SIF state

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1516	EC	sif_state	0	00	00000000	RO	0	0	SIF state

▷ **sif_state**

Master mode (VSYNC = '1 ') on the SIF (serial interface control block) indicates the status.

.

sif_state register(when master mode is on) :

1. 00h, 01h, 02h -> PC3089N is being initialized.
2. 03h -> initialization is done

(1517) Monitor switch

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1517	ED	monitor_switch	0	00	00000000	RO	0	0	Monitoring sampled switch level for embedded OSD control

▷ **monitor switch**

when sw_control0[2](sw_sel) = '0'(switch pad) ,

monitor_switch[5:3] = "001" -> sw1 on

"010" -> sw2on

"011" -> sw3 on

"100" -> sw4 on

"101" -> sw5 on

▶ Register Tables (Detailed) : Group H

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(1796~1807) CCIR656 control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1796	04	sync_blankEAV_f0	182	B6	10110110	RW	5	0	Blank EAV for field0 of CCIR656 data or blank EAV for frame data
1797	05	sync_blankSAV_f0	171	AB	10101011	RW	5	0	Blank EAV for field1 of CCIR656 data or blank EAV for frame data
1798	06	sync_activeEAV_f0	157	9D	10011101	RW	5	0	Active EAV for field0 of CCIR656 data or active EAV for frame data
1799	07	sync_activeSAV_f0	128	80	10000000	RW	5	0	Active EAV for field1 of CCIR656 data or active EAV for frame data
1800	08	sync_blankEAV_f1	241	F1	11110001	RW	5	0	blank EAV for field1 of CCIR656 data
1801	09	sync_blankSAV_f1	236	EC	11101100	RW	5	0	blank SAV for field1 of CCIR656 data
1802	0A	sync_activeEAV_f1	218	DA	11011010	RW	5	0	Active EAV for field1 of CCIR656 data
1803	0B	sync_activeSAV_f1	199	C7	11000111	RW	5	0	Active SAV for field1 of CCIR656 data
1804	0C	sync_CCIR_FF	255	FF	11111111	RW	5	0	CCIR data format
1805	0D	sync_CCIR_00	0	00	00000000	RW	5	0	
1806	0E	sync_CCIR_80	128	80	10000000	RW	5	0	
1807	0F	sync_CCIR_10	16	10	00010000	RW	5	0	

▷ CCIR656 sync index value

EAV and SAV data value for synchronization.

Address	Name	Description
05, 09h	*BlankSAV*	Blank Range Start of Video
04, 08h	*BlankEAV*	Blank Range End of Video
06, 0Ah	*ActiveEAV*	Active Range End of Video
07, 0Bh	*ActiveSAV*	Active Range Start of Video

▷ sync_ccirFF

CCIR data format FFh

▷ sync_ccir00

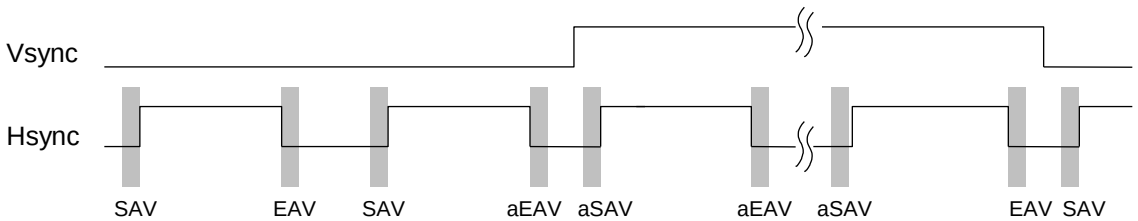
CCIR data format 00h

▷ sync_ccir80

CCIR data format 80h

▷ sync_ccir10

CCIR data format 10h



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... 80 10 80 10 80 10 80 10 FF 00 00 XY ... FF 00 00 XY 80 10 80 10 80 10 80 10

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(1813~1817) OSD transparency

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1813	15	osd_opac0	16	10	xxx10000	RW	5	0	OSD layer0 transparency
1814	16	osd_opac1	16	10	xxx10000	RW	5	0	OSD layer1 transparency
1815	17	osd_opac2	16	10	xxx10000	RW	5	0	OSD layer2 transparency
1816	18	osd_opac3	16	10	xxx10000	RW	5	0	OSD layer3 transparency
1817	19	hlight_opac	16	10	xxx10000	RW	5	0	Highlight zone transparency

▷ OSD transparency

The control range : 0~16d.

0d : transparency 100%, 16d : transparency 0%

▷ Hilight zone transparency

Through Hlight_opac register can control the transparency of the highlight zone.

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(1949) Encoder control 1

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1949	9D	enc_control1	0	00	00000000	RW	5	0	Encoder mode

register name : enc_control1								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
1949d (9Dh)	7	x	0	reserved				
	6	x	0	reserved				
	5	x	0	reserved				
	4	x	0	reserved				
	3	enc_chroma_kill	0	TV encoder chroma signal kill enable@led ON(BW_mode) 0b : disable 1b : enable				
	2	burst kill	0	TV encoder color burst kill enable@led ON(BW_mode) 0b : disable 1b : enable				
	1	x	0	reserved				
	0	x	0	reserved				

▷ **enc_chroma_kill**

When LED on, chroma signal kill can be set as enable or disable

▷ **burst_kill**

When LED on, burst signal kill can be set as enable or disable

(1953~1959) UTC data

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1953	A1	osd_init_s	18	12	00010010	RW	5	0	UTC data sampling control
1954	A2	pelco_sync_s	24	18	00011000	RW	5	0	
1955	A3	osd_init_w	4	04	xxx00100	RW	5	0	
1956	A4	pelco_efline_h	0	00	xxxxxx00	RW	5	0	
1957	A5	pelco_efline_l	19	13	00010011	RW	5	0	
1958	A6	pelco_ofline_h	0	00	xxxxxx00	RW	5	0	
1959	A7	pelco_ofline_l	19	13	00010011	RW	5	0	

▷ OSD init

After finishing burst signal, osd init signal is generated delay for pclk period of osd_init_s.

▷ Pelco sync

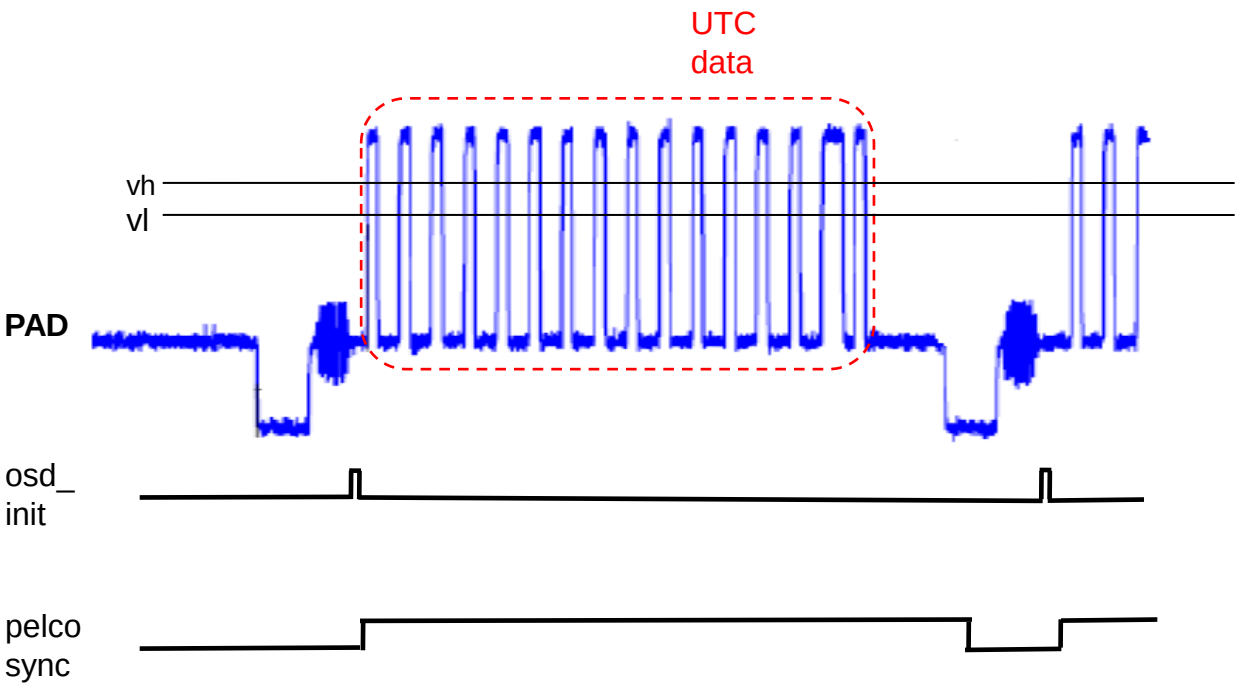
After finishing burst signal, pelco sync signal is generated delay for pclk period of pelco_sync_s
pelco_sync_s[7]=sign bit, pelco_sync[6:0]=magnitude

▷ OSD width

Determine width of osd init signal

▷ pelco line

It is show which number of signal is UTC data in each field.



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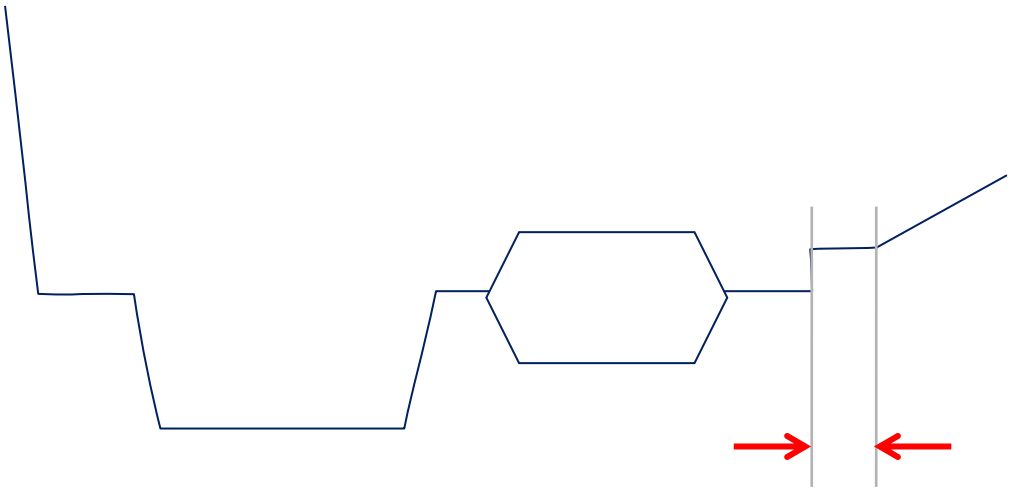
(1961) Setup time width

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1961	A9	setup_w	7	07	xxx00111	RW	5	0	Setup time width

▷ setup_w

Setup time width control register.



setup_w

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(1962~1966) horizontal sync control of composite signal

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1962	AA	hsync_p_toffset	0	00	xxx00000	RW	5	0	Stop point of hsync
1963	AB	burst_duration	0	00	00000000	RW	5	0	Burst duration
1964	AC	burst_slope_step	56	38	00111000	RW	5	0	
1965	AD	l_blank_start	0	00	00000000	RW	5	0	Line blanking interval
1966	AE	l_blank_stop	0	00	00000000	RW	5	0	

▷ **hsync_p_toffset**

Hsync stop point can be 1 clock(pclk)unit control.

▷ **burst_duration**

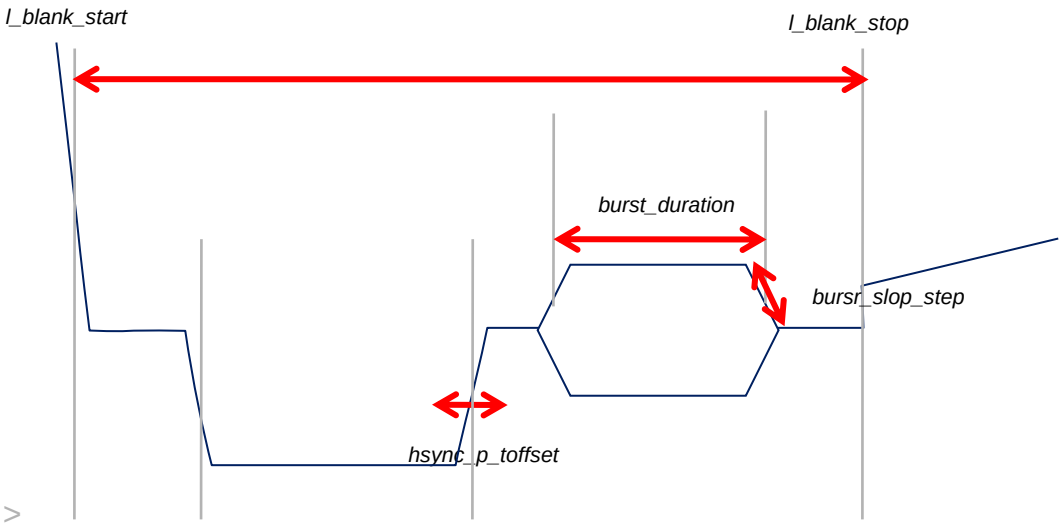
Burst duration can be 1 clock(pclk)unit control.

▷ **burst_slope_step**

Burst envelop rising or falling time can be 1 clock(pclk)unit control.

▷ **l_blank_start/stop**

Line blanking interval start/stop point control.



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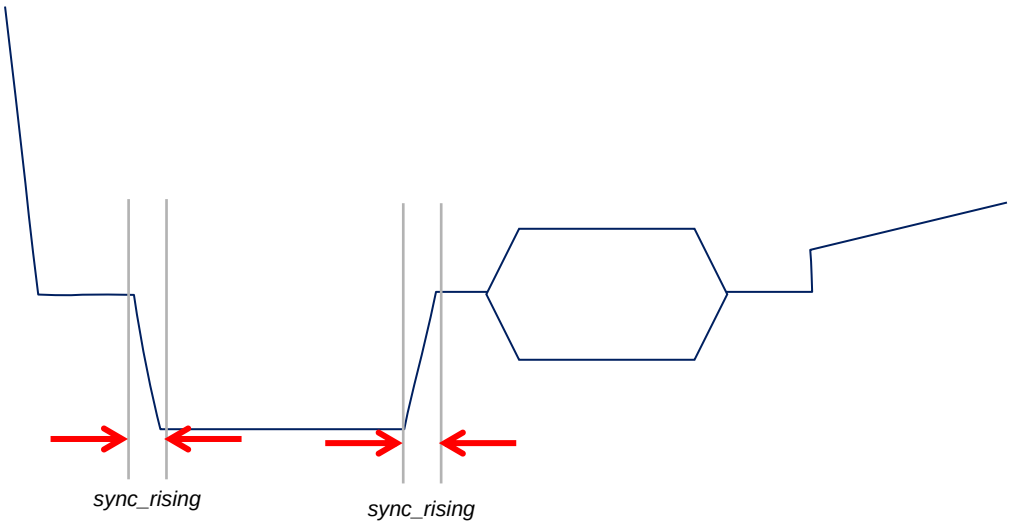
(1967) control rise time of composite horizontal sync

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1967	AF	sync_rising	1	01	xxxx0001	RW	5	0	horizontal rising time control of composite signal

▷ **sync_rising**

Horizontal sync rising time can be 0~15color(pclk)unit control.



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(1975) Encoder mode

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1975	B7	enc_mode	u	u	uuuuuuuu	RW	5	0	Encoder mode

▷ **enc_mode[1:0]**

"00" : (M) NTSC, NTSC-J, NTSC-4.43

"01" : (B, D, G, H, I, N) PAL

"10" : (Nc) PAL

"11" : (M) PAL

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(1976~1991) Composite level parameters

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1976	B8	enc_sync	16	10	00010000	RW	5	0	Encoder sync level
1977	B9	enc_blankH	0	00	00000000	RW	5	0	Encoder blank level
1978	BA	enc_blankL	u	u	uuuuuuuu	RW	5	0	
1979	BB	enc_pedestal	u	u	uuuuuuuu	RW	5	0	Encoder pedestal
1980	BC	enc_burst	u	u	uuuuuuuu	RW	5	0	Burst amplitude
1981	BD	enc_Ygain	u	u	uuuuuuuu	RW	5	0	Y convergence gain from YCbCr to YUV
1982	BE	enc_Ugain	u	u	uuuuuuuu	RW	5	0	U convergence gain from YCbCr to YUV
1983	BF	enc_Vgain	u	u	uuuuuuuu	RW	5	0	V convergence gain from YCbCr to YUV
1984	C0	enc_Yrange_H	3	03	xxxxx011	RW	5	0	Max. luminance
1985	C1	enc_Yrange_L	32	20	00100000	RW	5	0	
1986	C2	enc_Crange_H	1	01	xxxxx001	RW	5	0	Max. amplitudes of chrominance
1987	C3	enc_Crange_L	u	u	uuuuuuuu	RW	5	0	
1988	C4	enc_chroma_max_H	3	03	xxxxx011	RW	5	0	Maximum chrominance of composite output
1989	C5	enc_chroma_max_L	u	u	uuuuuuuu	RW	5	0	
1990	C6	enc_chroma_min_H	0	00	xxxxx000	RW	5	0	Minimum chrominance of composite output
1991	C7	enc_chroma_min_L	u	u	uuuuuuuu	RW	5	0	

▷ ***enc_sync***

Encoder sync level

▷ ***enc_blank***

Encoder blank level

▷ ***enc_pedestal***

Encoder pedestal level

▷ ***enc_burst***

Burst amplitude

▷ ***enc_Y/U/Vgain***

Conversion gain of YCbCr to YUV

▷ ***enc_Yrange***

Separate Y range into positive and negative regions.

▷ ***enc_Crange***

Define maximum level of Chrominance.

▷ ***enc_chroma_max***

Define maximum level of Composite.

▷ ***enc_chroma_min***

Define minimum level of Composite.

default value : U ➔ wire-strapping register

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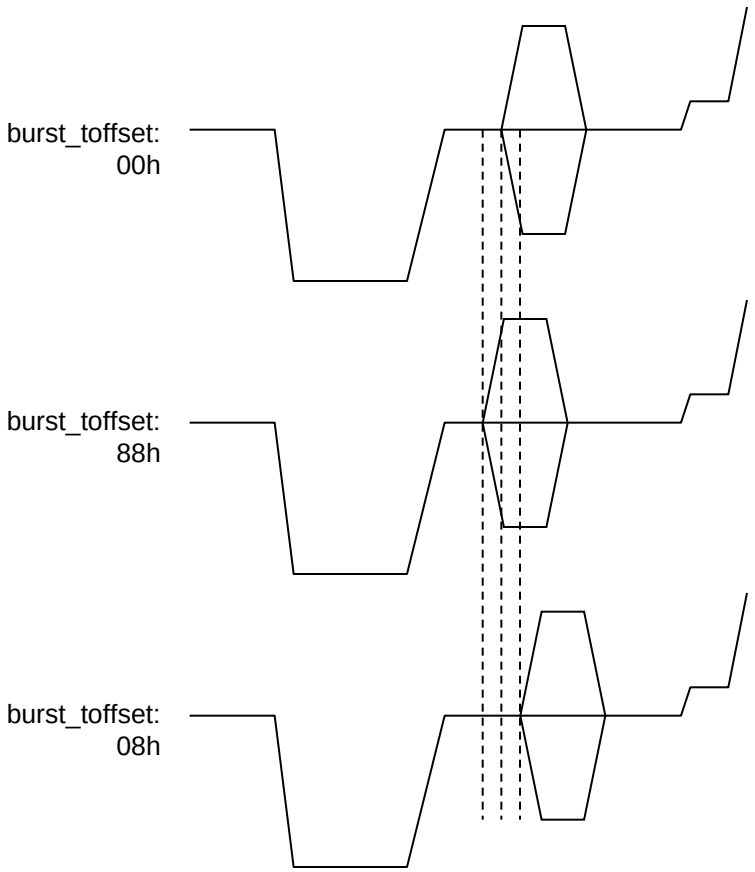
(2029) Burst time offset

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
2029	E6	burst_toffset	0	00	00000000	RW	5	0	Burst time +/- offset

▷ **burst_toffset**

Change the location of the color burst.
msb: sign, other bits : magnitude



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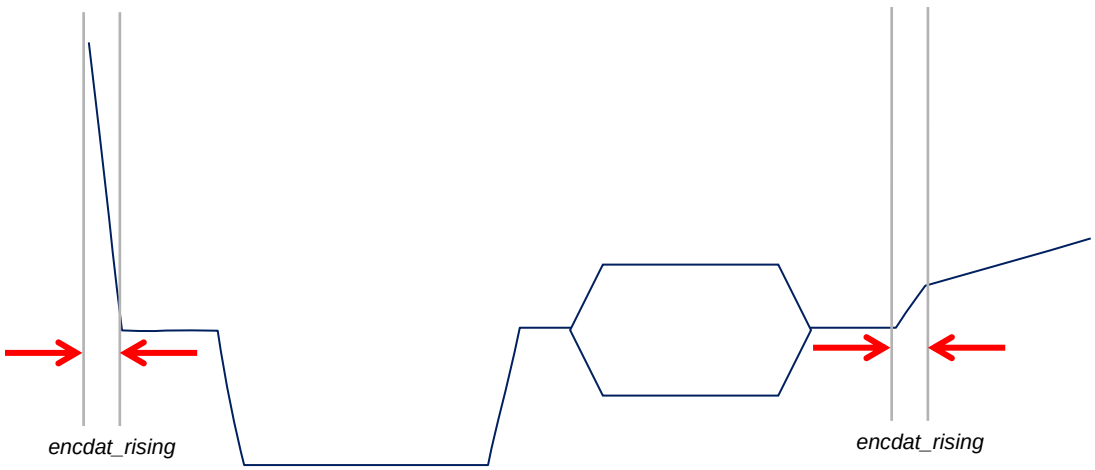
(2034) control rise time of composite horizontal sync

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
2034	EB	encdat_rising	1	01	xxxx0001	RW	5	0	edge of the line blanking pulse rising time control

▷ **encdat_rising**

edge of the line blanking pulse rising time can be 0~15 clock(pclk)unit control.



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(2035) Sub-carrier frequency control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
2035	EC	enc_scfreq	u	u	uuuuuuuu	RW	5	0	Subcarrier frequency selection for which TV mode

▷ **enc_scfreq**

default value : U ➔ wire-strapping register

Subcarrier frequency selection for which TV mode.

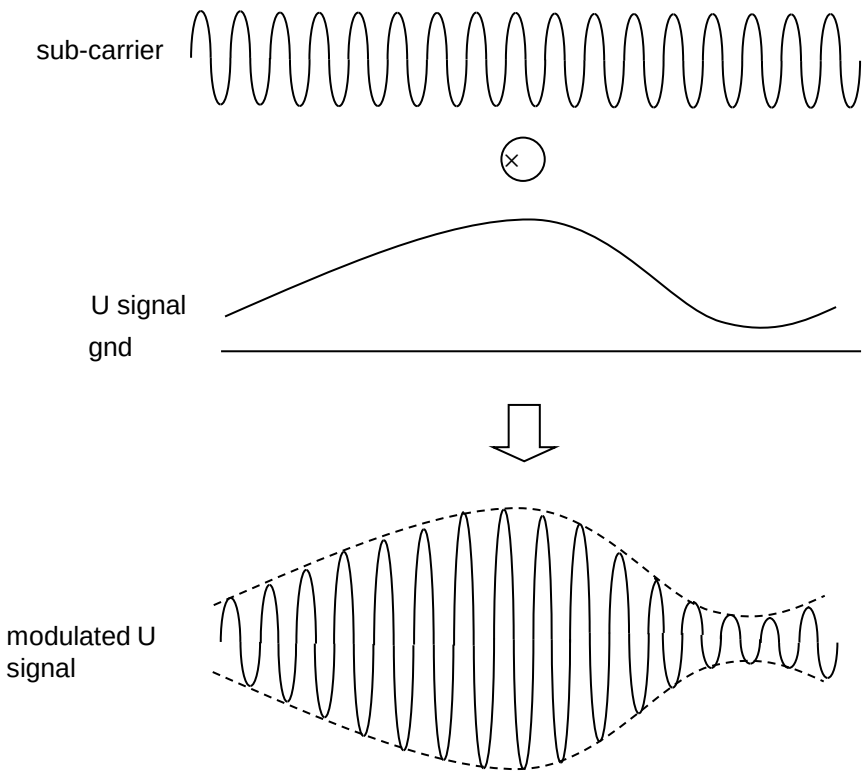
"00" : 3.579545 MHz for (M) NTSC, NTSC-J

"01" : 4.43361875 MHz for (B, D, G, H, I, N) PAL

"10" : 3.58205625 MHz for (Nc) PAL

"11" : 3.57561149 MHz for (M) PAL

$C = U*\sin(\omega t) + V*\cos(\omega t)$



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